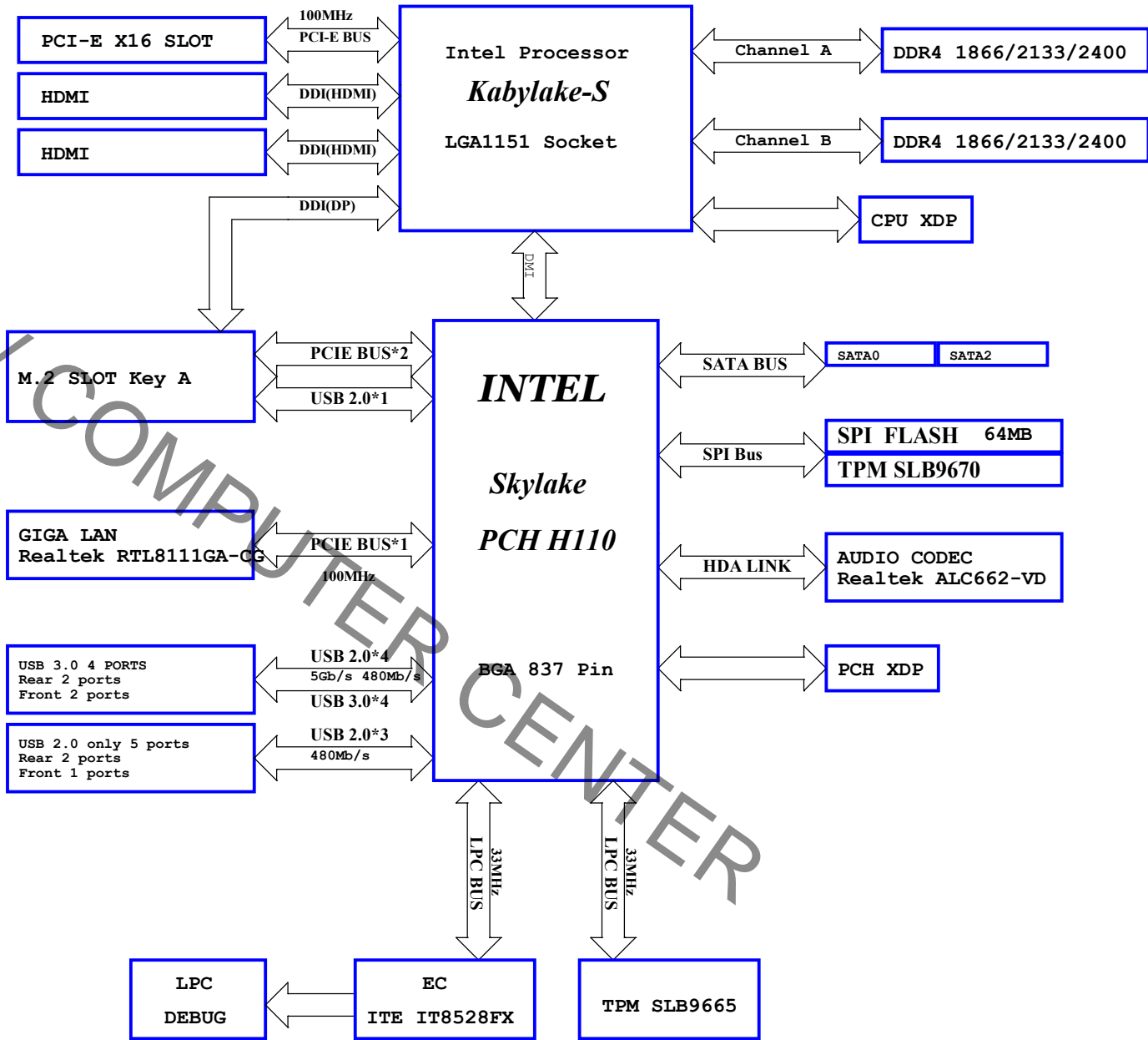
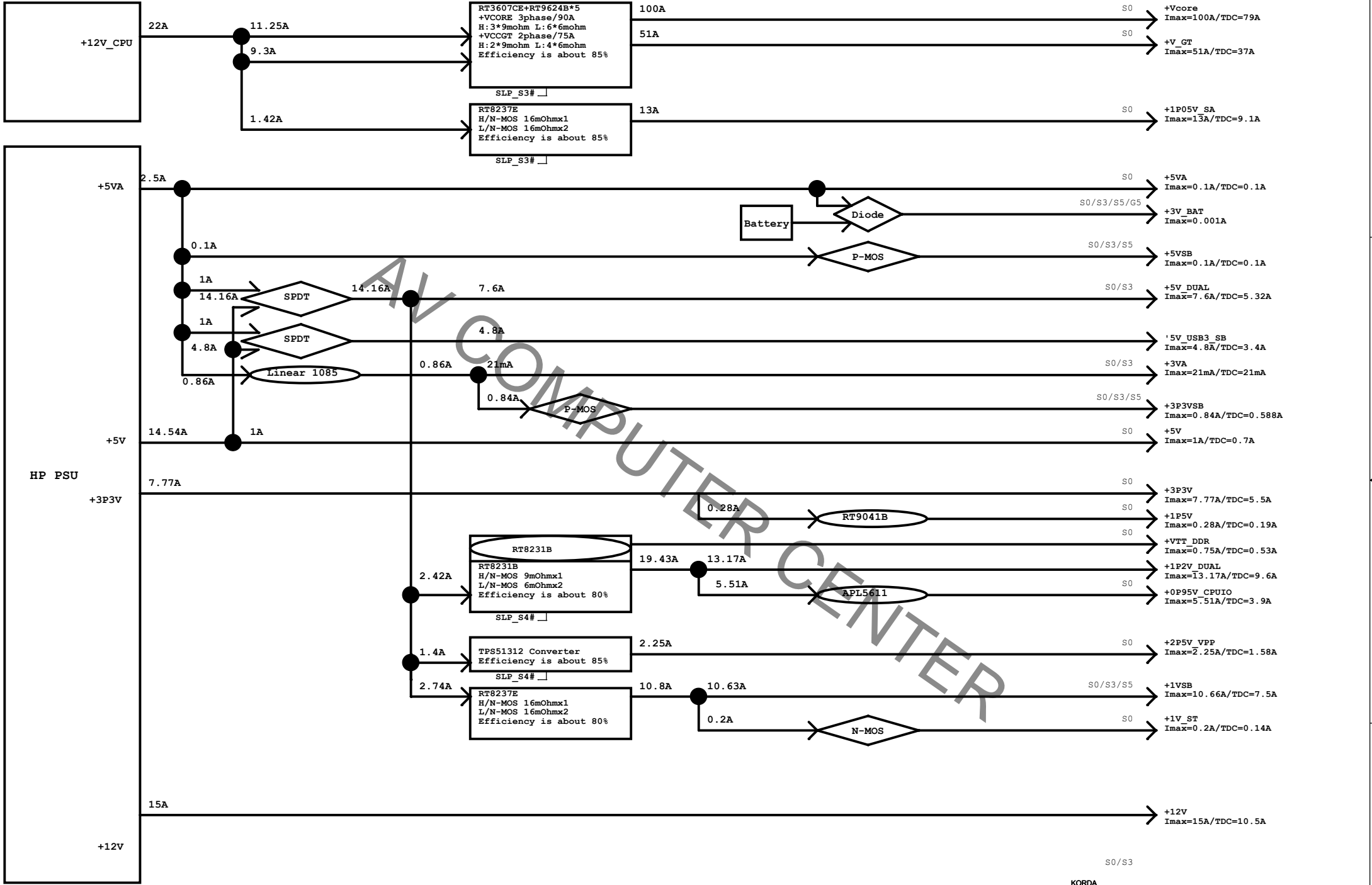


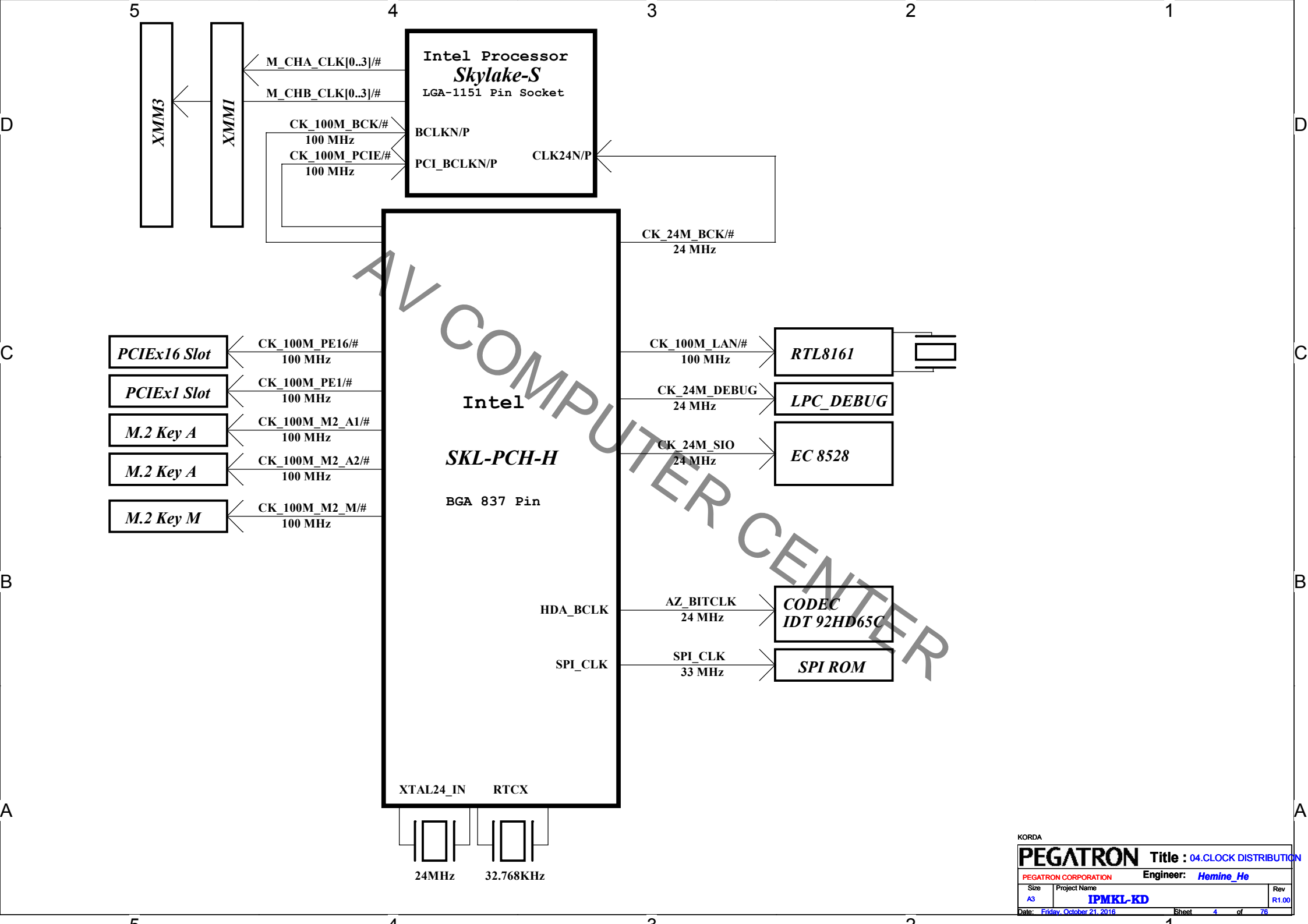
PAGE		TITLE
01		BLOCK DIAGRAM
02		CHANGE HISTORY
03		Power Diagram
04		Clock Distribution
05		Power Sequence
06		POWER DISTRIBUTION
07~12		CPU
13~16		DDR4
17		DDR4 TERMINATION A&B
18~25		PCH
26		RSMRST#
27		PCH DPWROK
28		X16 SLOT
29		X1 SLOT
30		M.2 Key A
31		Reserved
32~33		HDMI
34		AUDIO CODEC
35		AUDIO Header
36		AUDIO CONNECTOR
37		XXXXX
38		USB 2.0 Header
39		RJ45+USB2.0
40		USB3.0 Header
41		Rear USB2.0
42		Rear USB3.0
43		RTL8161
44		Reserved
45		EC 8528
46		CHASSIS LED
47		SATA Connector
48		SERIAL HEADER
49		Fan Circuit
50		LED
51		SMBUS/SPI
52		RTC/CMOS
53		LPC DEBUG1
54		FRONT PANEL
55		SCREW
56		XDP
57		ATX POWER
58~62		Vcore & VCCGT
63		+1P05V_SA
64		+0P95V_CPUIO
65		VDDQ
66		VPP
67		+1VSB
68		+1V_ST
69		VA/SB
70		+5V_DUAL/+5V_USB3_SB
71		EMI CAP
72		+1P5V
73~74		HDMI Level shift
75~76		TYPE-C Header & CYPD 2122

AV COMPUTER CENTER

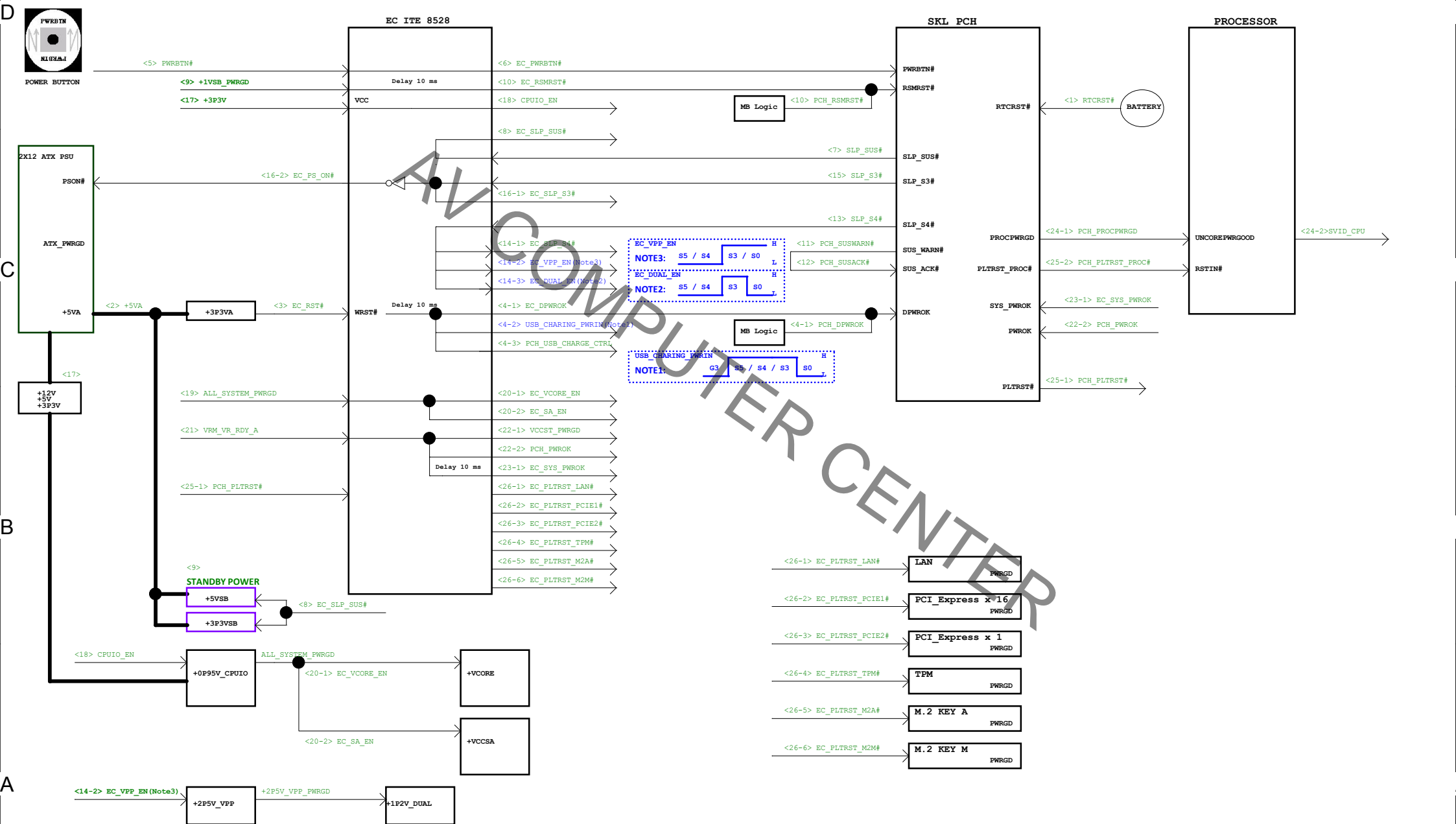


Version	Date	Comments	Page	Version	Date	Comments	Page
1.00	2/16	First release.					
	3/17	Meet DVT BOM.					
1.01	4/12	Add net SPI_WP_EC to EC GPF3.	P.45				
		Power team Bom change.	P.58				
		Audio design change.	P. 34.35				
		Crystal SR45 10M ohm size change.	P.23				
		PR350 change to small symbol.	P.65				
		Type-C header P459 change to RA.	P.75				
	4/18	Change UC1 to 499ohm.	P.38				
		Change RFC28 to 499ohm.	P.40				
		Change P1CB8 to 499ohm.	P.57				
		Change ECC19 to 100P.	P.45				
		Change SR337 to 1000P.	P.22				
		Add ESD to USB2.0, USB3.0 ports.					
		Reserve PR351 330ohm for 3P3VSB.	P.69				
		Add 90 ohm choke for USB2.0 ports.					
	4/21	Add OC circuit for Type-C.	P.75				
	4/25	Reserve 10uF for type-C VBUS.	P.75				
	4/26	Bom change from NI to I for OC SR753, SR128.	P.19				
		Installed HC24 1000pF.	P.10				
		Change Board ID to PVT1.	P.45				
		Change LAD from 15ohm to 33ohm.	P.20				
		Install ECR93.	P.45				
	5/17	Change OC# voltage divider resistor (UR11,UR13,UR15,UR17)from 10K ohm to 8.2K.	P.19				
	6/3	Add UC72 4.7uF for OC.	P.75				
		Install UL26, UL28 for RF issue.	P.75				
		Change Board ID to PVT2.	P.45				
	6/16	Install SR752, remove SR742.	P.22				





ODENSE2 POWER SEQUENCE MAP



	CPU Skylake-S 42
+VCORE	-> 100A (Imax) - 95W
+0P95V_CPUIO	-> 5.51A (Imax) - W
+1P05V_SA	-> 13A (Imax) - W
+V_AXG	-> 51A (Imax) - W

	PCH
+1VSB	-> 10.97A - W
+3P3V	-> 0.2A - W
+3P3VSB	-> 0.27A - W
+3P3VA	-> 0.021A - W
+BATT	RTC (G3) -> 6uA - 0.0198mW

	DDR4 DIMM (4) & Termination
+1P2V_DUAL	-> 19.4 A - W
+VPP (2.5V)	-> 2.25 A - W
+VTT_DDR(0.75V)	-> 0.75A - 0.56W

	PCI Express x 1
+12V	-> 5A - 60W
+3P3V	-> 3.0A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	PCI Express x 16
+12V	-> 5.5A - 66W
+3P3V	-> 3.0A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	LAN RTL8161
+3P3VSB	-> 165mA - 538mW

	EC IT8528E
+3P3V	-> mA - mW

	ALC3863-CG
+3P3V	-> mA - mW

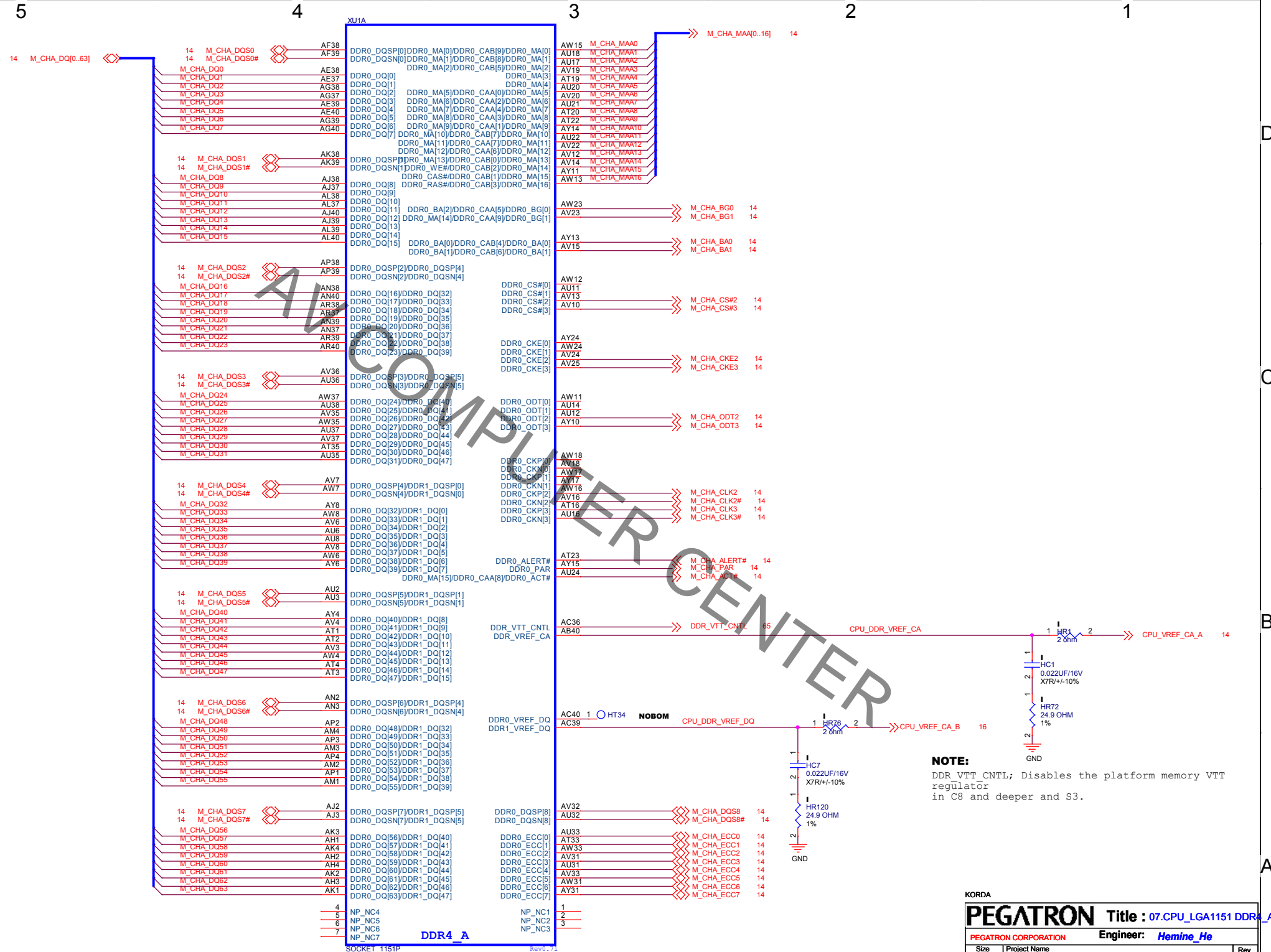
+5V_DUAL	USB2.0 8 PORTS/USB3.0 4 PORTS (S0, S1) ->8A - 40W
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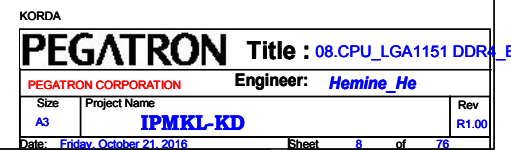
	M.2
+3P3V	-> 2A - W

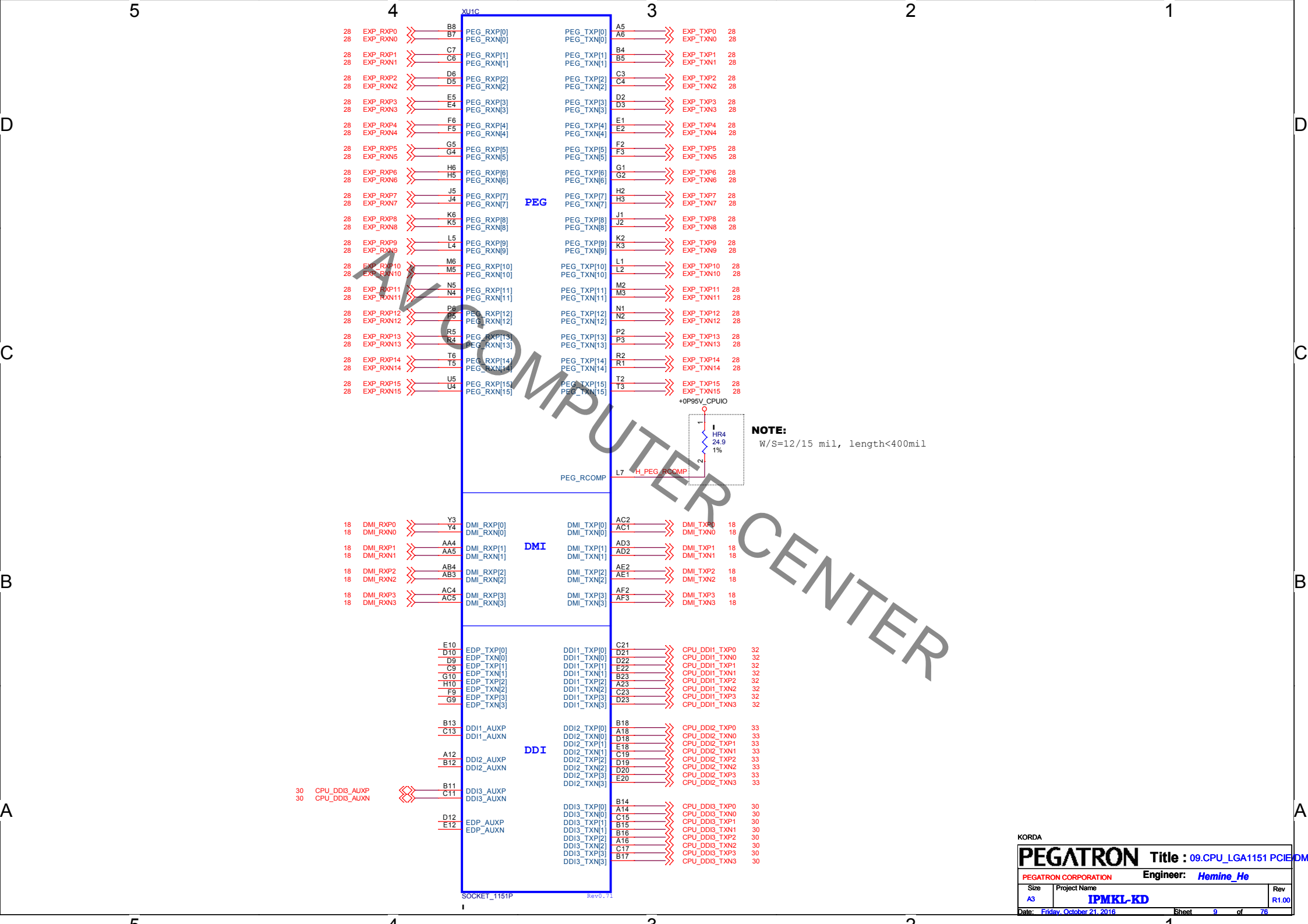
	HDMI1
+5V	-> mA - mW -> mA - mW

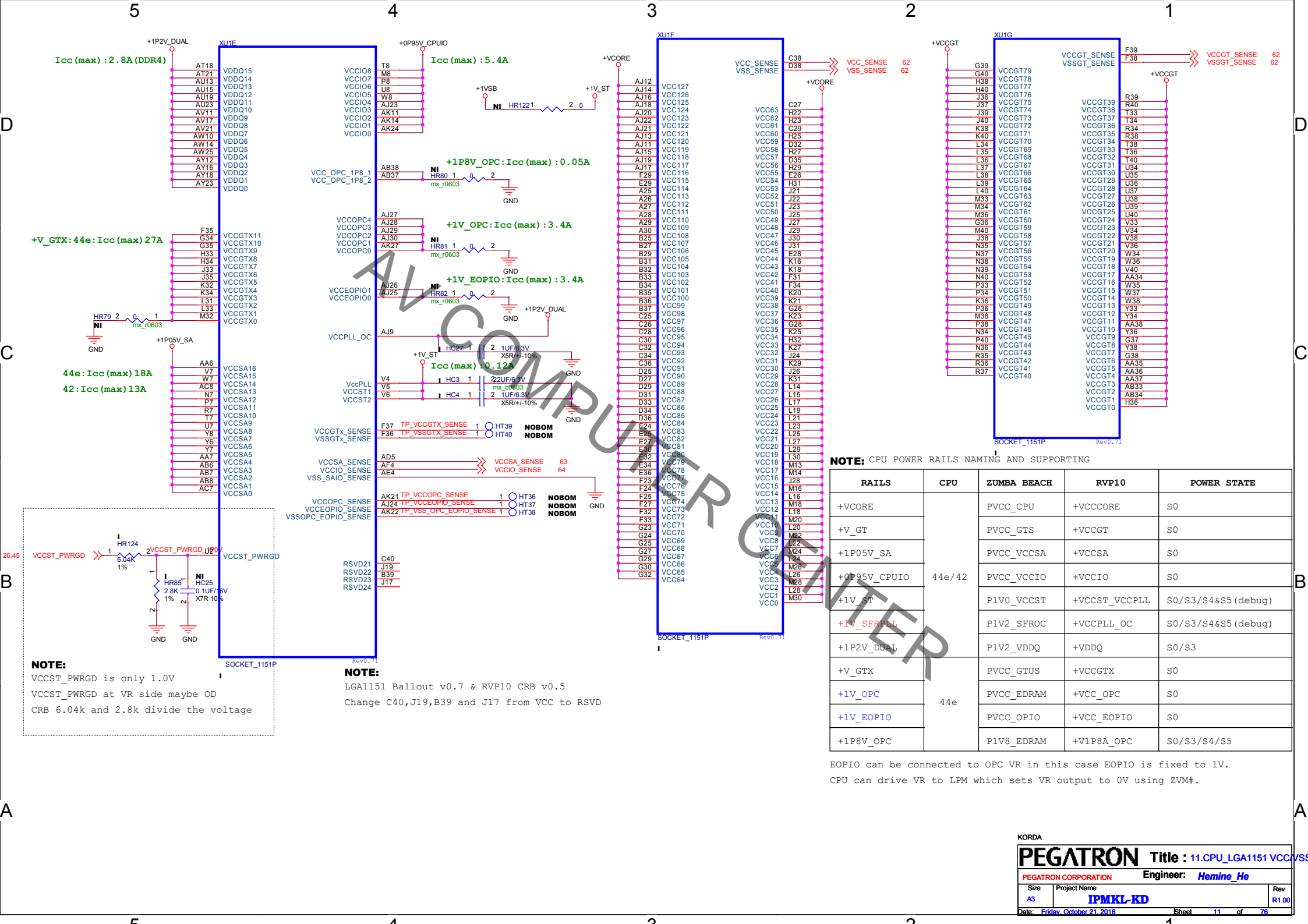
	HDMI2
+5V	-> mA - mW -> mA - mW

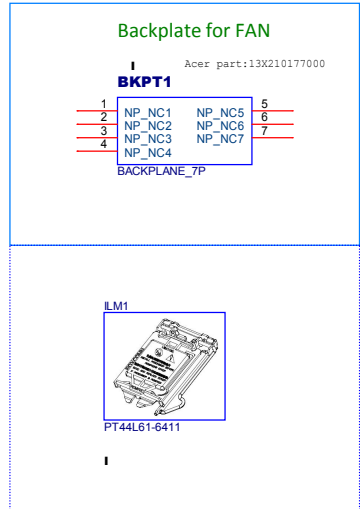
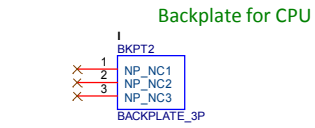
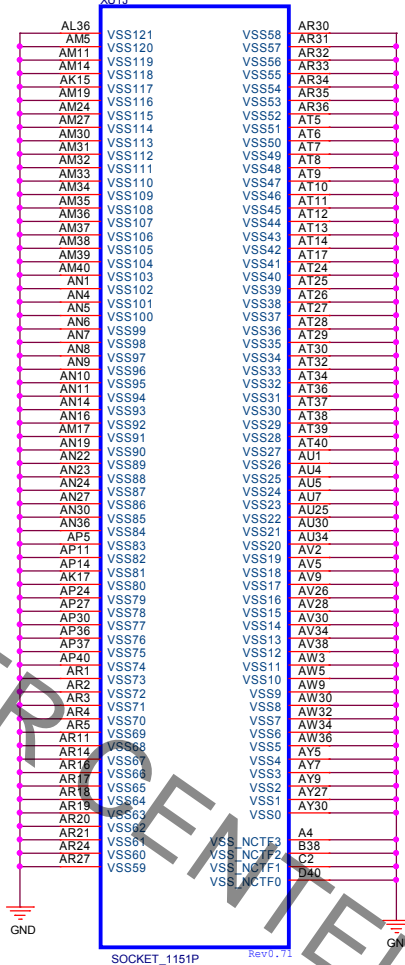
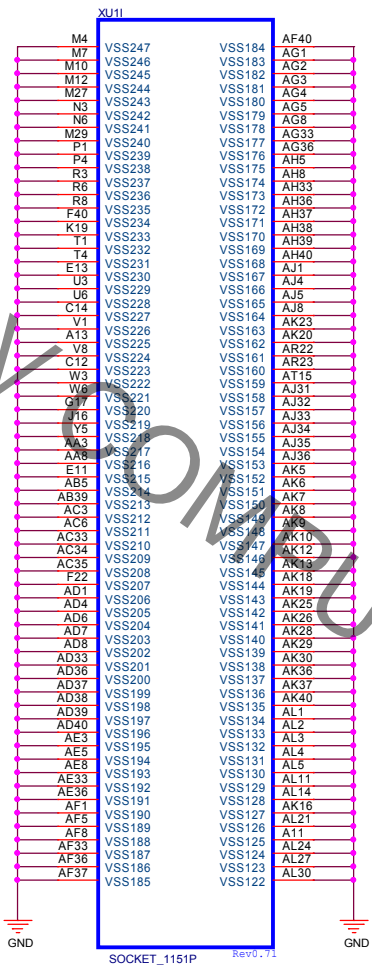
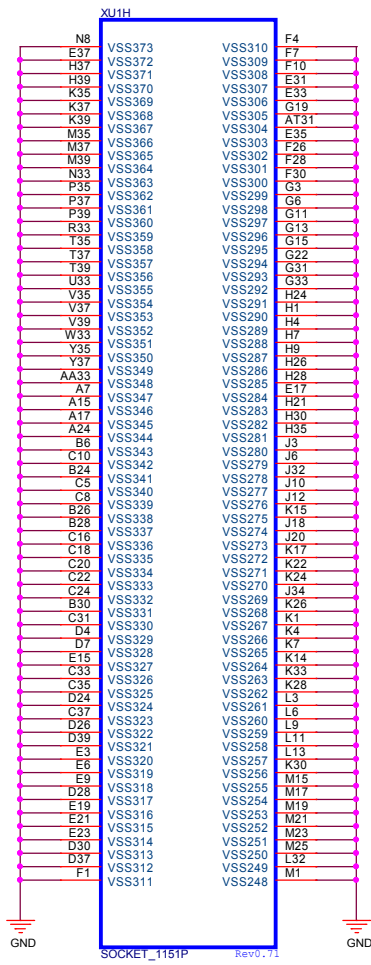
	FANS
+12V	-> 1.2A - 14.4W





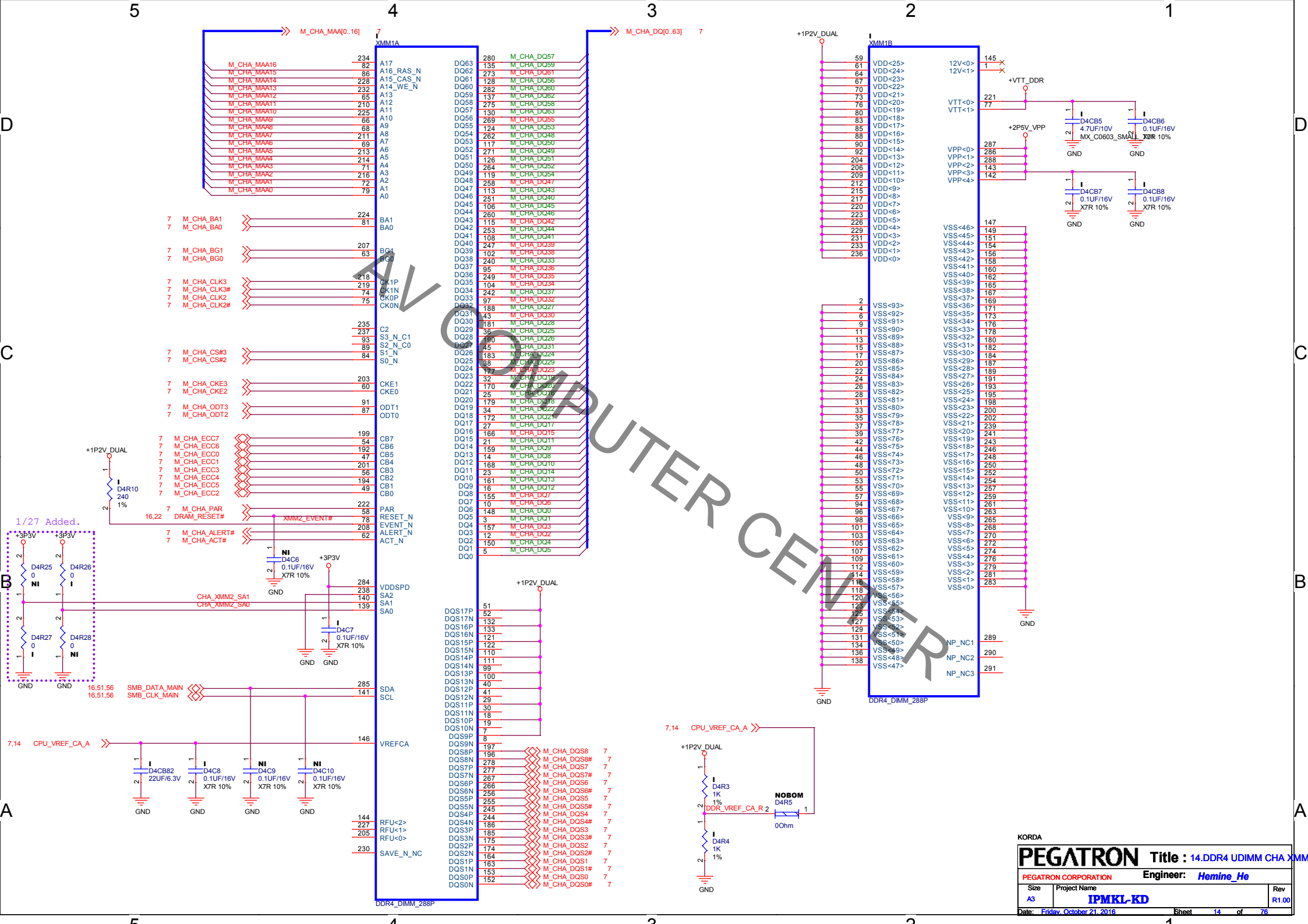


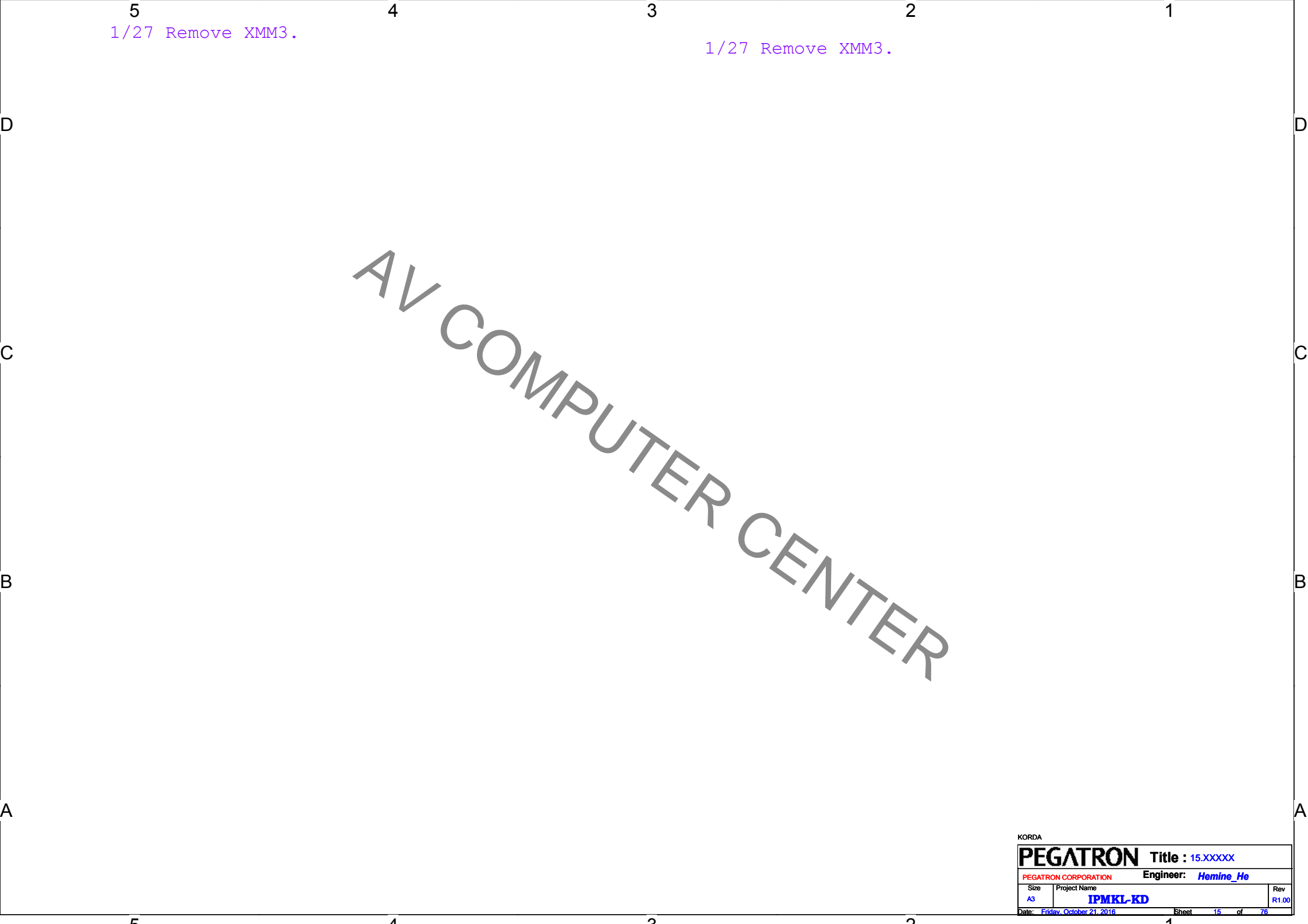




AV COMPUTER CENTER

KORDA		
PEGATRON		Title : 13.XXXXX
PEGATRON CORPORATION		Engineer: Hemine_He
Size A3	Project Name IPMKL-KD	Rev R1.00
Date: Friday, October 21, 2016		
Sheet 13 of 76		



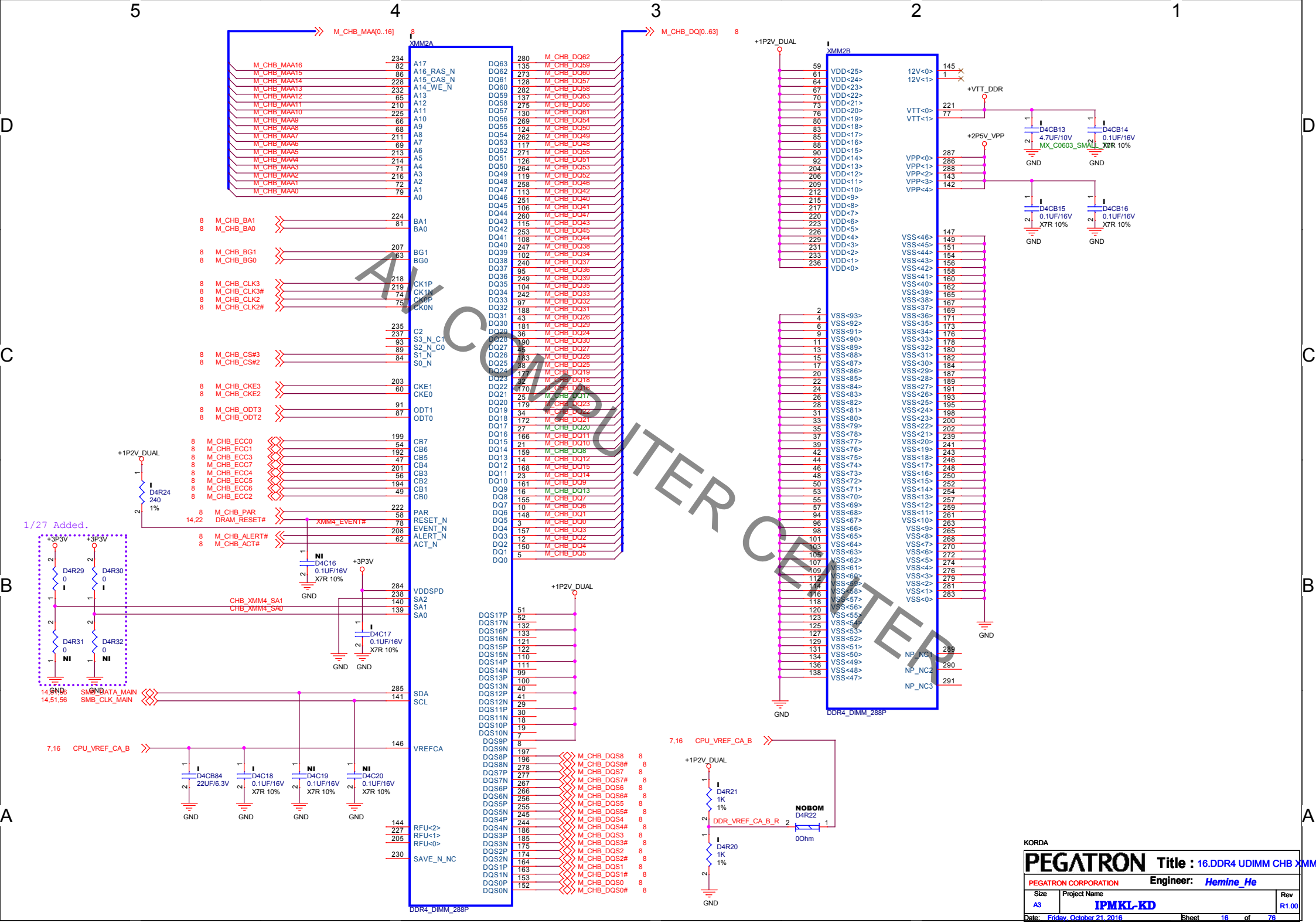


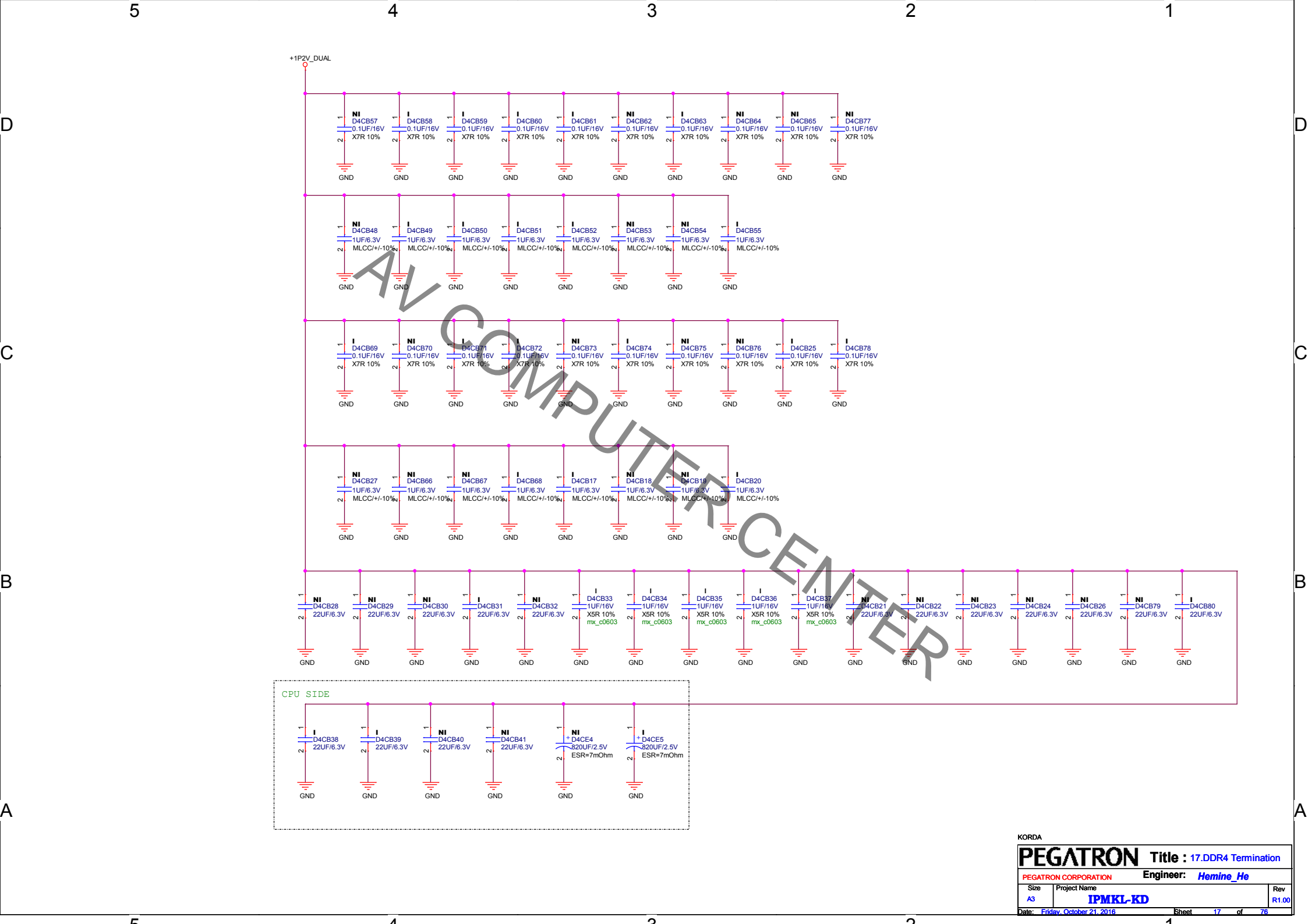
5
1/27 Remove XMM3.

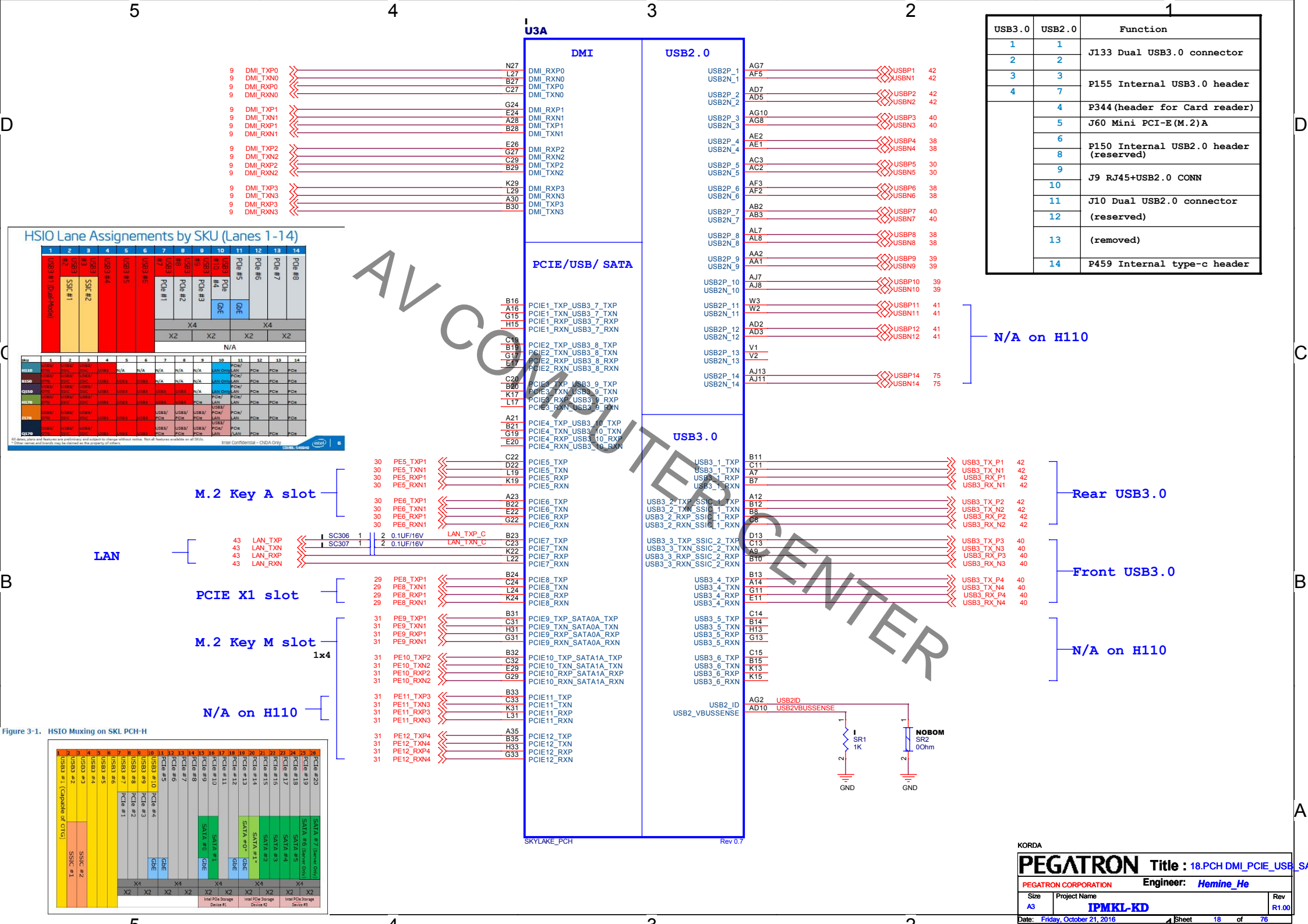
3
1/27 Remove XMM3.

AV COMPUTER CENTER

KORDA		
PEGATRON		Title : 15.XXXXX
PEGATRON CORPORATION		Engineer: Hemine_He
Size A3	Project Name IPMKL-KD	Rev R1.00
Date: Friday, October 21, 2016		
Sheet 15 of 76		







High: requests SATA device to enter into the DEVSLP power state
Low: SATA device to exit from the DEVSLP power state and transition to active state
When used as DEVSLP, no external PU or PD required from SATA Host DEVSLP.

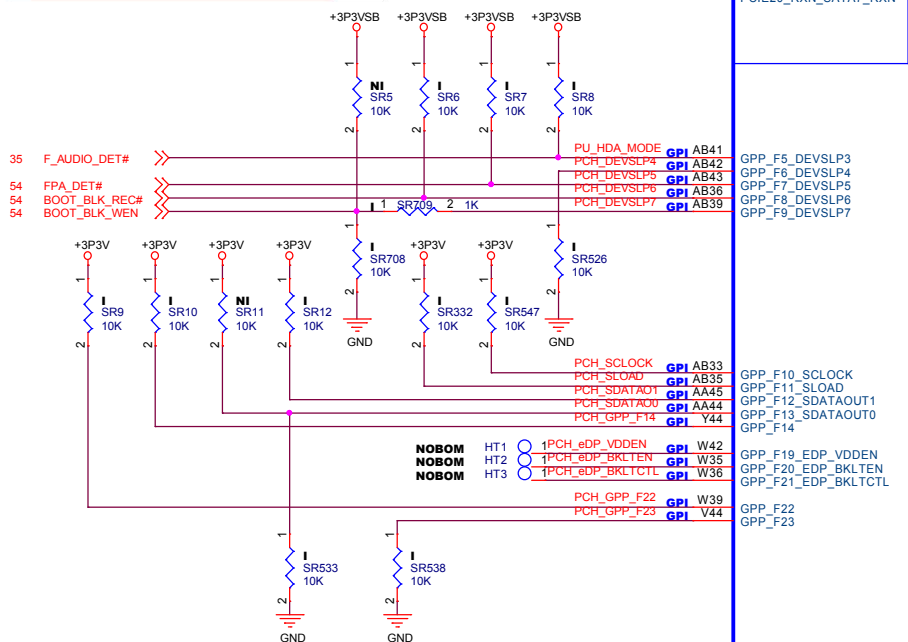
PCIE/SATA



HSIO Lane Assignments by SKU (Lanes 15-26)

15	16	17	18	19	20	21	22	23	24	25	26
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SA1A #1	SA1A #2	SA1A #3	SA1A #4	SA1A #5	SA1A #6	SA1A #7	SA1A #8	SA1A #9	SA1A #10	SA1A #11	
SA1B #1	SA1B #2	SA1B #3	SA1B #4	SA1B #5	SA1B #6	SA1B #7	SA1B #8	SA1B #9	SA1B #10	SA1B #11	
SA1C #1	SA1C #2	SA1C #3	SA1C #4	SA1C #5	SA1C #6	SA1C #7	SA1C #8	SA1C #9	SA1C #10	SA1C #11	
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SA3N #1	SA3N #2	SA3N #3	SA3N #4	SA3N #5	SA3N #6	SA3N #7	SA3N #8	SA3N #9	SA3N #10	SA3N #11	
SA3O #1	SA3O #2	SA3O #3	SA3O #4	SA3O #5	SA3O #6	SA3O #7	SA3O #8	SA3O #9	SA3O #10	SA3O #11	
SA3P #1	SA3P #2	SA3P #3	SA3P #4	SA3P #5	SA3P #6	SA3P #7	SA3P #8	SA3P #9	SA3P #10	SA3P #11	
SA3Q #1	SA3Q #2	SA3Q #3	SA3Q #4	SA3Q #5	SA3Q #6	SA3Q #7	SA3Q #8	SA3Q #9	SA3Q #10	SA3Q #11	
SA3R #1	SA3R #2	SA3R #3	SA3R #4	SA3R #5	SA3R #6	SA3R #7	SA3R #8	SA3R #9	SA3R #10	SA3R #11	
SA3S #1	SA3S #2	SA3S #3	SA3S #4	SA3S #5	SA3S #6	SA3S #7	SA3S #8	SA3S #9	SA3S #10	SA3S #11	
SA3T #1	SA3T #2	SA3T #3	SA3T #4	SA3T #5	SA3T #6	SA3T #7	SA3T #8	SA3T #9	SA3T #10	SA3T #11	
SA3U #1	SA3U #2	SA3U #3	SA3U #4	SA3U #5	SA3U #6	SA3U #7	SA3U #8	SA3U #9	SA3U #10	SA3U #11	
SA3V #1	SA3V #2	SA3V #3	SA3V #4	SA3V #5	SA3V #6	SA3V #7	SA3V #8	SA3V #9	SA3V #10	SA3V #11	
SA3W #1	SA3W #2	SA3W #3	SA3W #4	SA3W #5	SA3W #6	SA3W #7	SA3W #8	SA3W #9	SA3W #10	SA3W #11	
SA3X #1	SA3X #2	SA3X #3	SA3X #4	SA3X #5	SA3X #6	SA3X #7	SA3X #8	SA3X #9	SA3X #10	SA3X #11	
SA3Y #1	SA3Y #2	SA3Y #3	SA3Y #4	SA3Y #5	SA3Y #6	SA3Y #7	SA3Y #8	SA3Y #9	SA3Y #10	SA3Y #11	
SA3Z #1	SA3Z #2	SA3Z #3	SA3Z #4	SA3Z #5	SA3Z #6	SA3Z #7	SA3Z #8	SA3Z #9	SA3Z #10	SA3Z #11	
SA4A #1	SA4A #2	SA4A #3	SA4A #4	SA4A #5	SA4A #6	SA4A #7	SA4A #8	SA4A #9	SA4A #10	SA4A #11	
SA4B #1	SA4B #2	SA4B #3	SA4B #4	SA4B #5	SA4B #6	SA4B #7	SA4B #8	SA4B #9	SA4B #10	SA4B #11	
SA4C #1	SA4C #2	SA4C #3	SA4C #4	SA4C #5	SA4C #6	SA4C #7	SA4C #8	SA4C #9	SA4C #10	SA4C #11	
SA4D #1	SA4D #2	SA4D #3	SA4D #4	SA4D #5	SA4D #6	SA4D #7	SA4D #8	SA4D #9	SA4D #10	SA4D #11	
SA4E #1	SA4E #2	SA4E #3	SA4E #4	SA4E #5	SA4E #6	SA4E #7	SA4E #8	SA4E #9	SA4E #10	SA4E #11	
SA4F #1	SA4F #2	SA4F #3	SA4F #4	SA4F #5	SA4F #6	SA4F #7	SA4F #8	SA4F #9	SA4F #10	SA4F #11	
SA4G #1	SA4G #2	SA4G #3	SA4G #4	SA4G #5	SA4G #6	SA4G #7	SA4G #8	SA4G #9	SA4G #10	SA4G #11	
SA4H #1	SA4H #2	SA4H #3	SA4H #4	SA4H #5	SA4H #6	SA4H #7	SA4H #8	SA4H #9	SA4H #10	SA4H #11	
SA4I #1	SA4I #2	SA4I #3	SA4I #4	SA4I #5	SA4I #6	SA4I #7	SA4I #8	SA4I #9	SA4I #10	SA4I #11	
SA4J #1	SA4J #2	SA4J #3	SA4J #4	SA4J #5	SA4J #6	SA4J #7	SA4J #8	SA4J #9	SA4J #10	SA4J #11	
SA4K #1	SA4K #2	SA4K #3	SA4K #4	SA4K #5	SA4K #6	SA4K #7	SA4K #8	SA4K #9	SA4K #10	SA4K #11	
SA4L #1	SA4L #2	SA4L #3	SA4L #4	SA4L #5	SA4L #6	SA4L #7	SA4L #8	SA4L #9	SA4L #10	SA4L #11	
SA4M #1	SA4M #2	SA4M #3	SA4M #4	SA4M #5	SA4M #6	SA4M #7	SA4M #8	SA4M #9	SA4M #10	SA4M #11	
SA4N #1	SA4N #2	SA4N #3	SA4N #4	SA4N #5	SA4N #6	SA4N #7	SA4N #8	SA4N #9	SA4N #10	SA4N #11	
SA4O #1	SA4O #2	SA4O #3	SA4O #4	SA4O #5	SA4O #6	SA4O #7	SA4O #8	SA4O #9	SA4O #10	SA4O #11	
SA4P #1	SA4P #2	SA4P #3	SA4P #4	SA4P #5	SA4P #6	SA4P #7	SA4P #8	SA4P #9	SA4P #10	SA4P #11	
SA4Q #1	SA4Q #2	SA4Q #3	SA4Q #4	SA4Q #5	SA4Q #6	SA4Q #7	SA4Q #8	SA4Q #9	SA4Q #10	SA4Q #11	
SA4R #1	SA4R #2	SA4R #3	SA4R #4	SA4R #5	SA4R #6	SA4R #7	SA4R #8	SA4R #9	SA4R #10	SA4R #11	
SA4S #1	SA4S #2	SA4S #3	SA4S #4	SA4S #5	SA4S #6	SA4S #7	SA4S #8	SA4S #9	SA4S #10	SA4S #11	
SA4T #1	SA4T #2	SA4T #3	SA4T #4	SA4T #5	SA4T #6	SA4T #7	SA4T #8	SA4T #9	SA4T #10	SA4T #11	
SA4U #1	SA4U #2	SA4U #3	SA4U #4	SA4U #5	SA4U #6	SA4U #7	SA4U #8	SA4U #9	SA4U #10	SA4U #11	
SA4V #1	SA4V #2	SA4V #3	SA4V #4	SA4V #5	SA4V #6	SA4V #7	SA4V #8	SA4V #9	SA4V #10	SA4V #11	
SA4W #1	SA4W #2	SA4W #3	SA4W #4	SA4W #5	SA4W #6	SA4W #7	SA4W #8	SA4W #9	SA4W #10	SA4W #11	
SA4X #1	SA4X #2	SA4X #3	SA4X #4	SA4X #5	SA4X #6	SA4X					

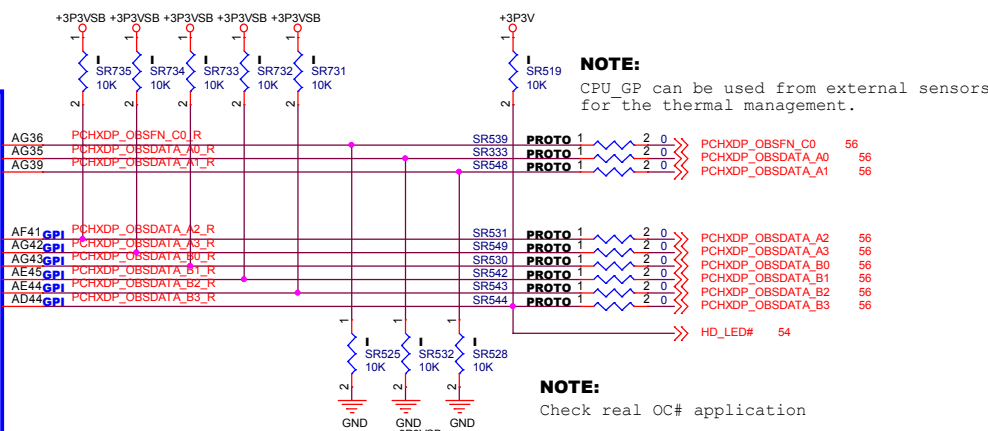
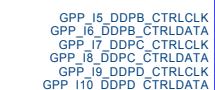
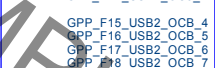
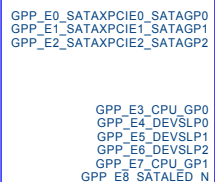
N/A on H110-



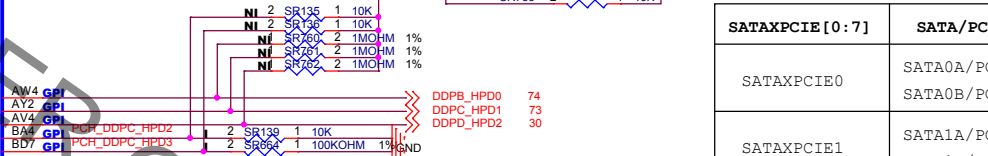
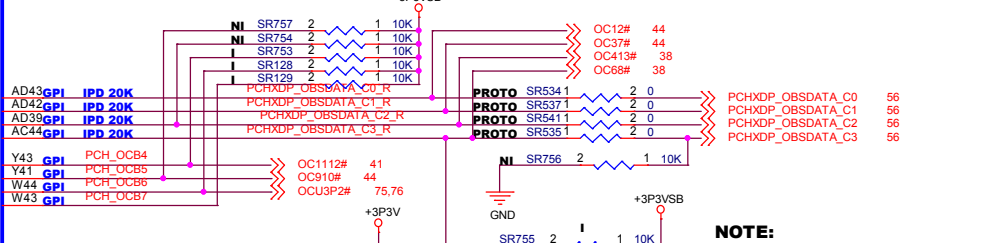
GPP F[11:10] for SWITCH#0 to select source from ISH or HOST

SKYLAKE_PCH

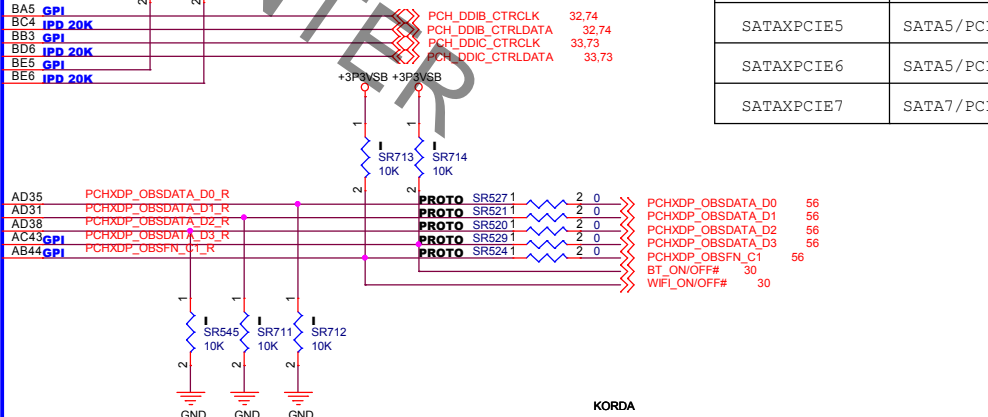
Rev 0.7



NOTE:
Check real OC# application



NOTE:	
SATAXPCIE[0:7]	SATA/PCIE
SATAXPCIE0	SATA0A/PCIE9 SATA0B/PCIE13
SATAXPCIE1	SATA1A/PCIE10 SATA1B/PCIE14
SATAXPCIE2	SATA2/PCIE15
SATAXPCIE3	SATA3/PCIE16
SATAXPCIE4	SATA4/PCIE17
SATAXPCIE5	SATA5/PCIE18
SATAXPCIE6	SATA5/PCIE19
SATAXPCIE7	SATA7/PCIE20



KORDA

PEGATRON Title : 19.PCH SATA/PCIE 2-8

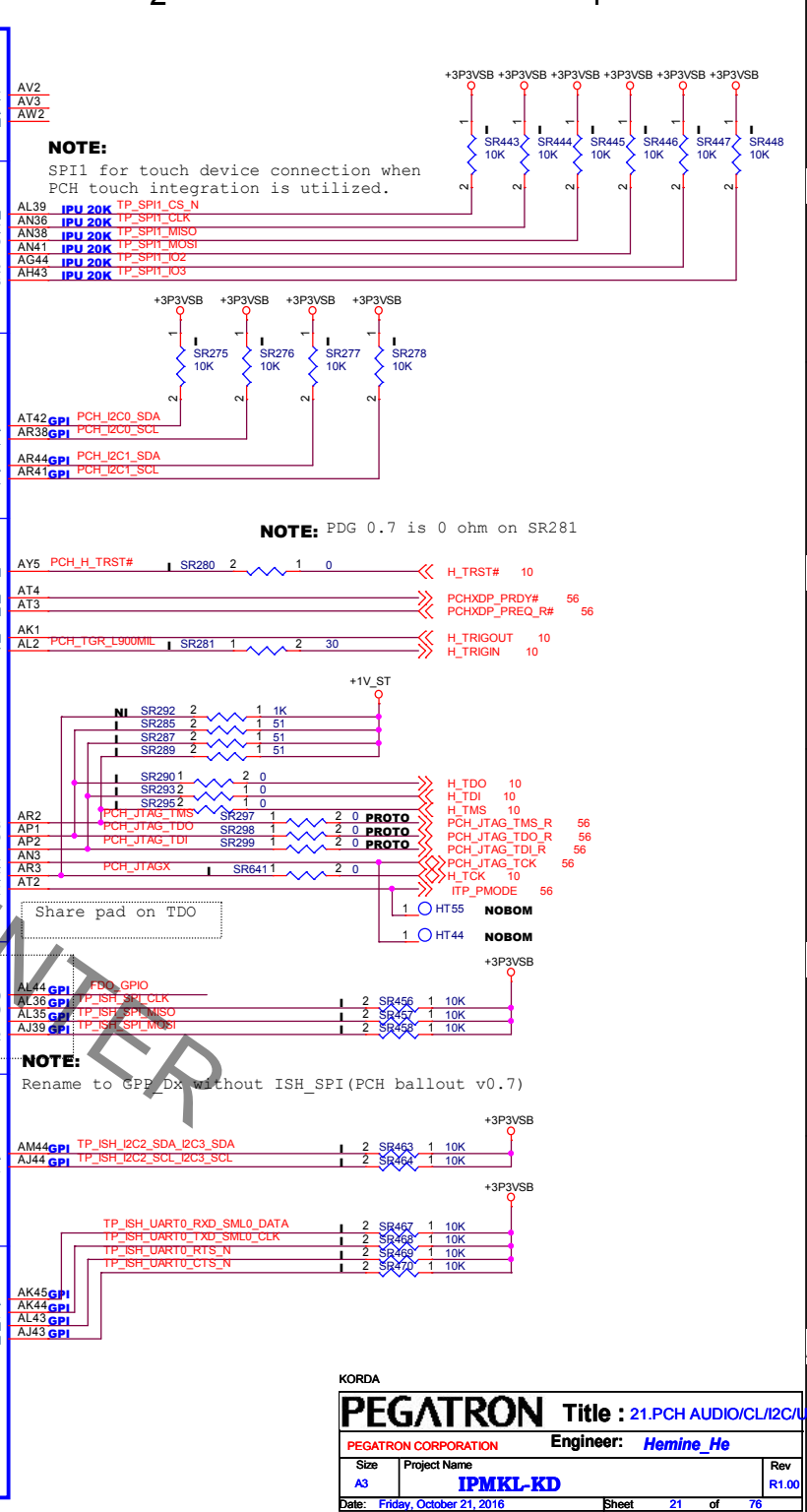
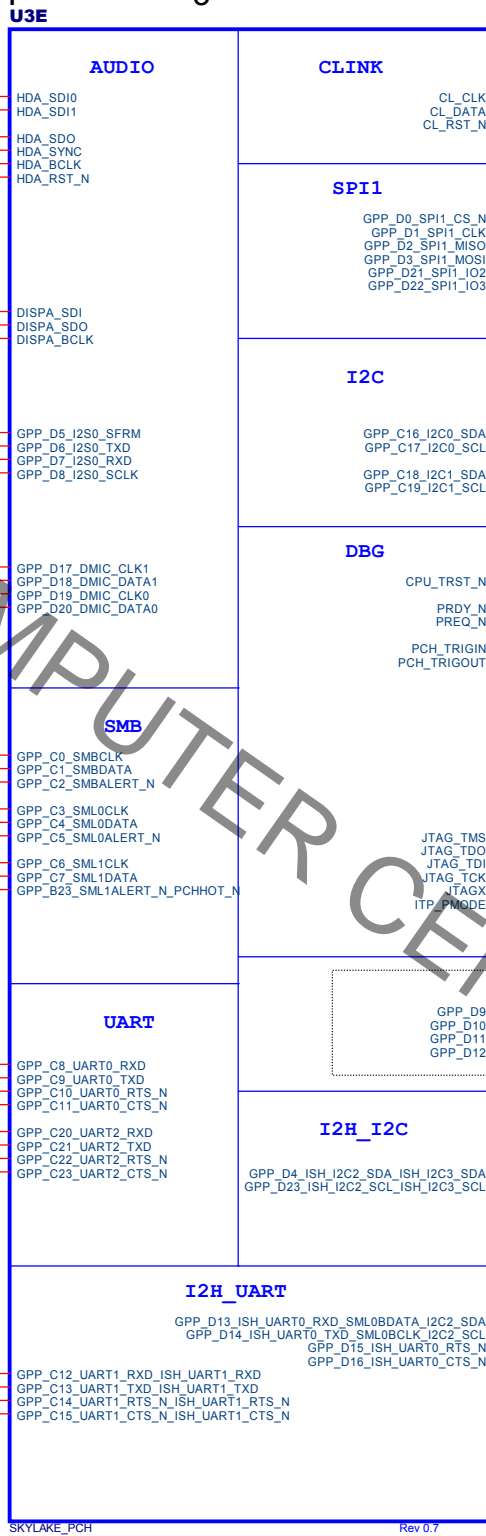
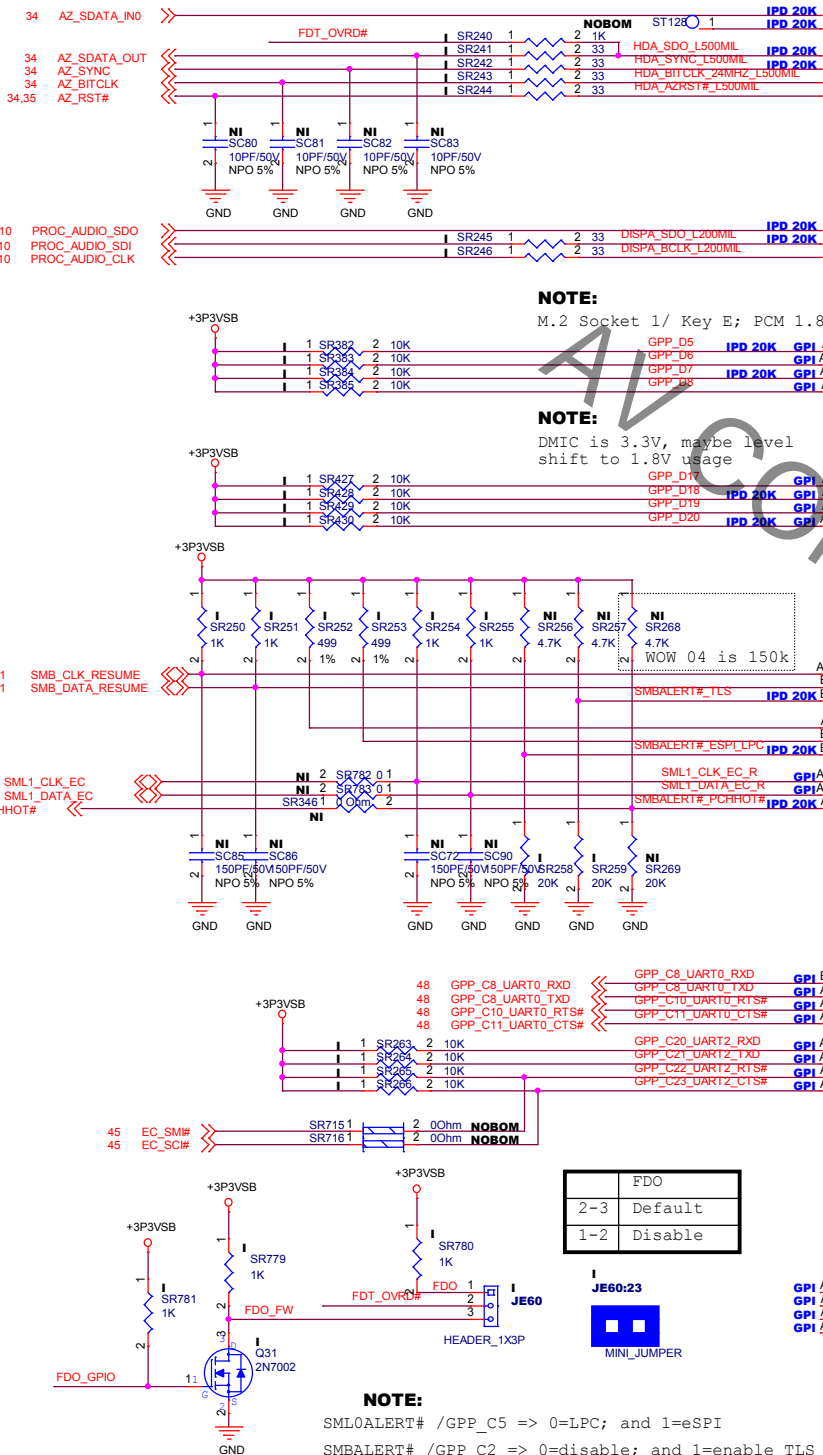
Engineer: Hemine He

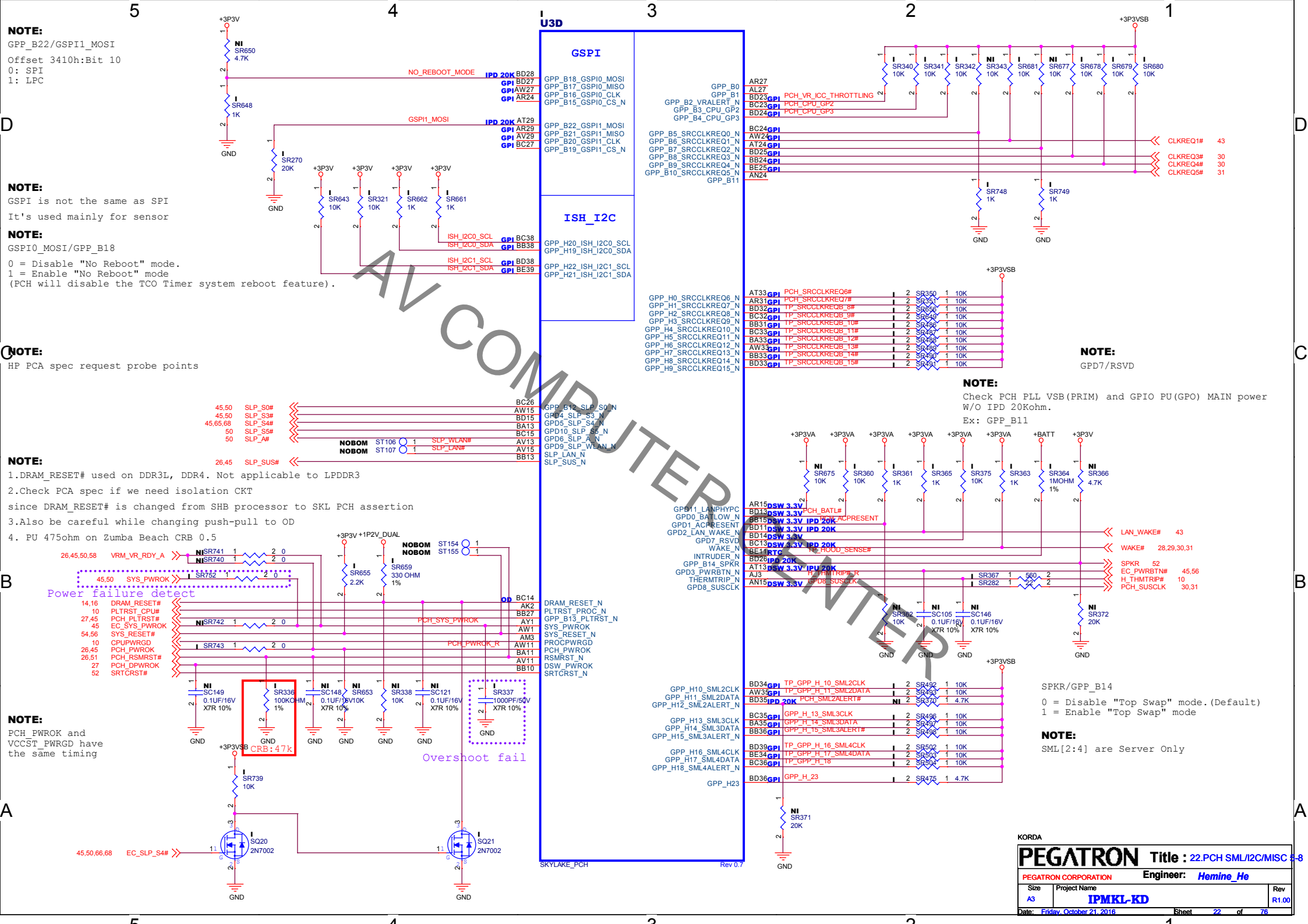
Size	Project Name	Rev
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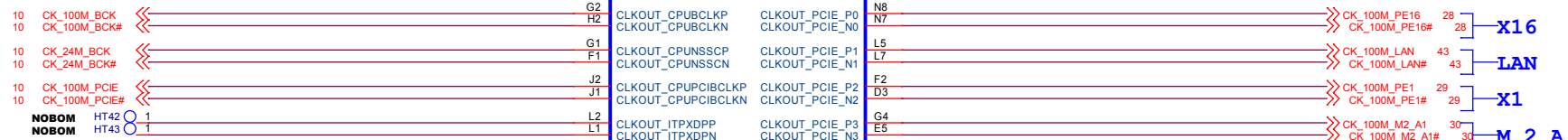
A3	IPMKL-KD	R1.00
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Date: Friday, October 21, 2016 Cited: 20 of 70

NOTE:
Check HDA_SDO or AZA_SDO_SSP0_TXD to support
Flash Descriptor Security Override/ME Debug Mode





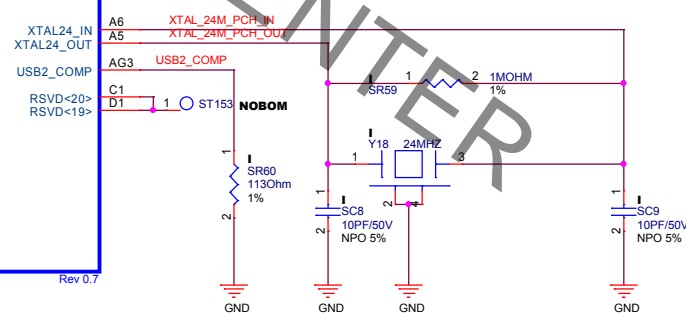
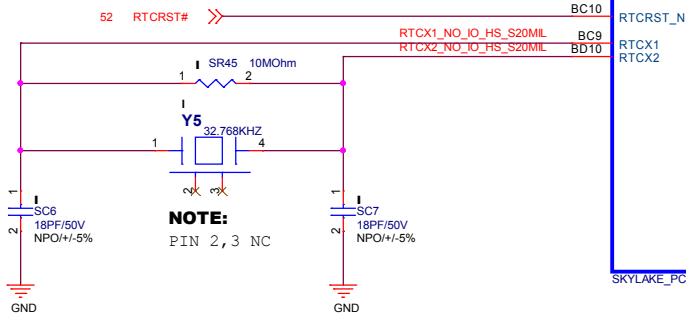
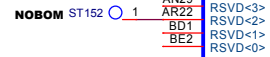
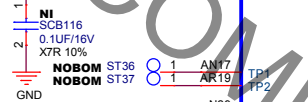
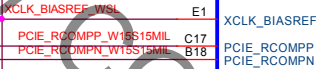
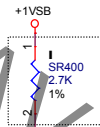
**NOTE:**

CRB: 2.71Kohm

Refer to GND; NOT near switching noise; spacing 3x

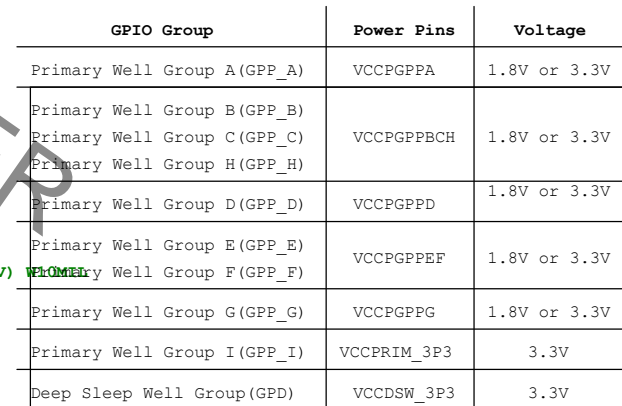
Add a GND shield(Width>4 mils)

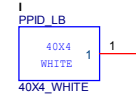
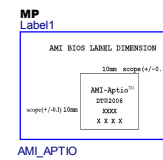
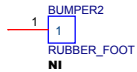
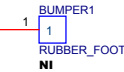
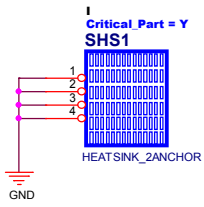
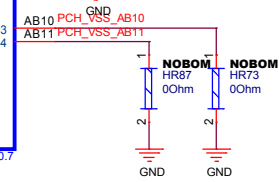
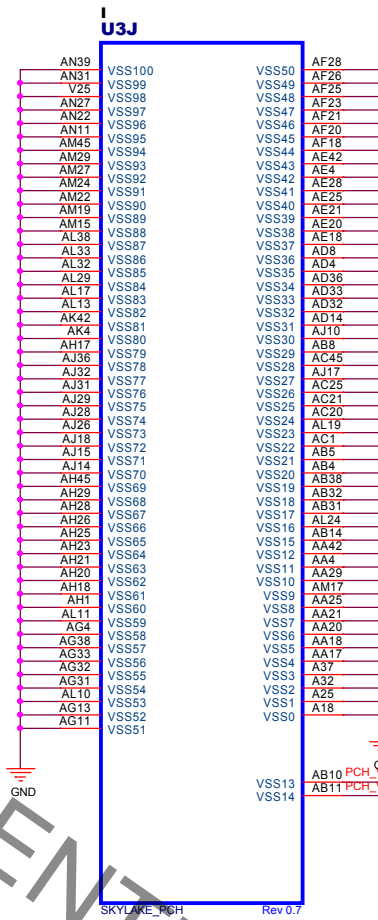
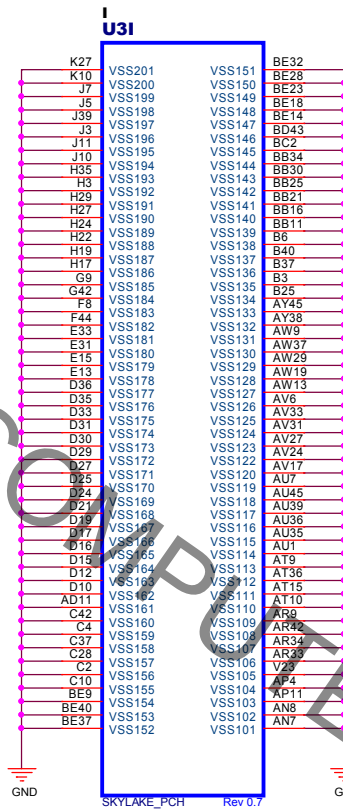
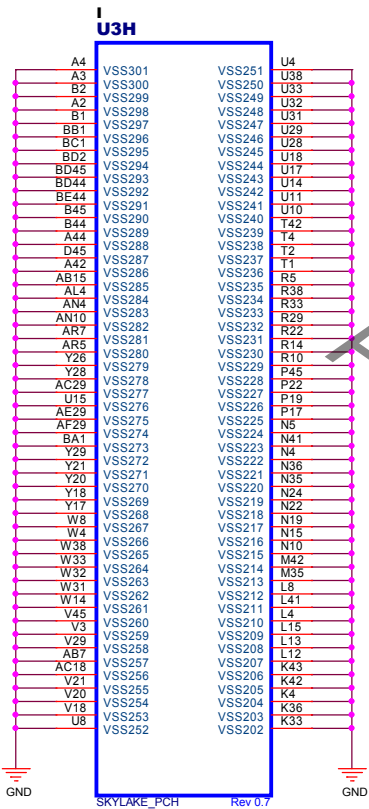
between XCLK_BIASREF and adjacent IO signals



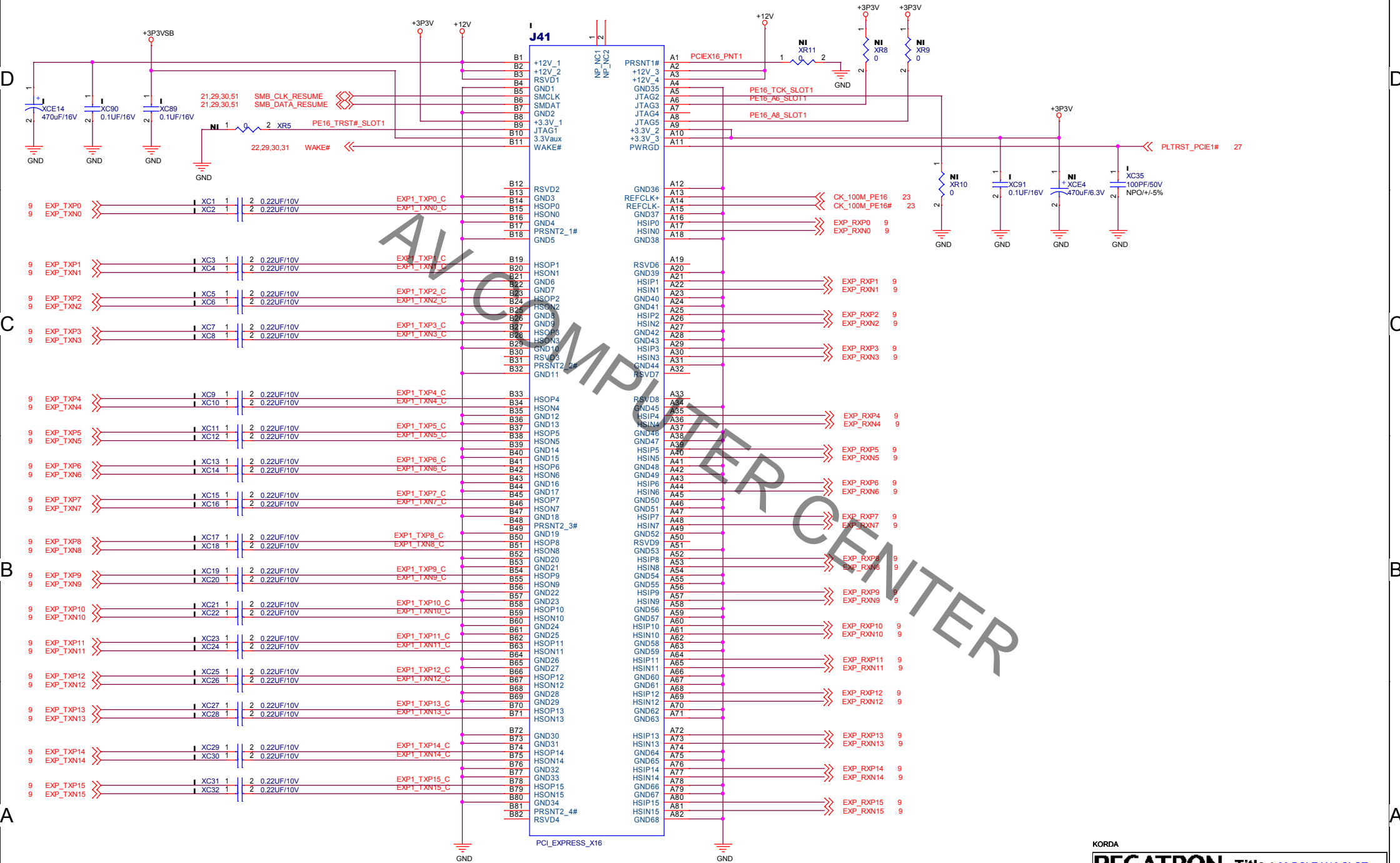
KORDA

A

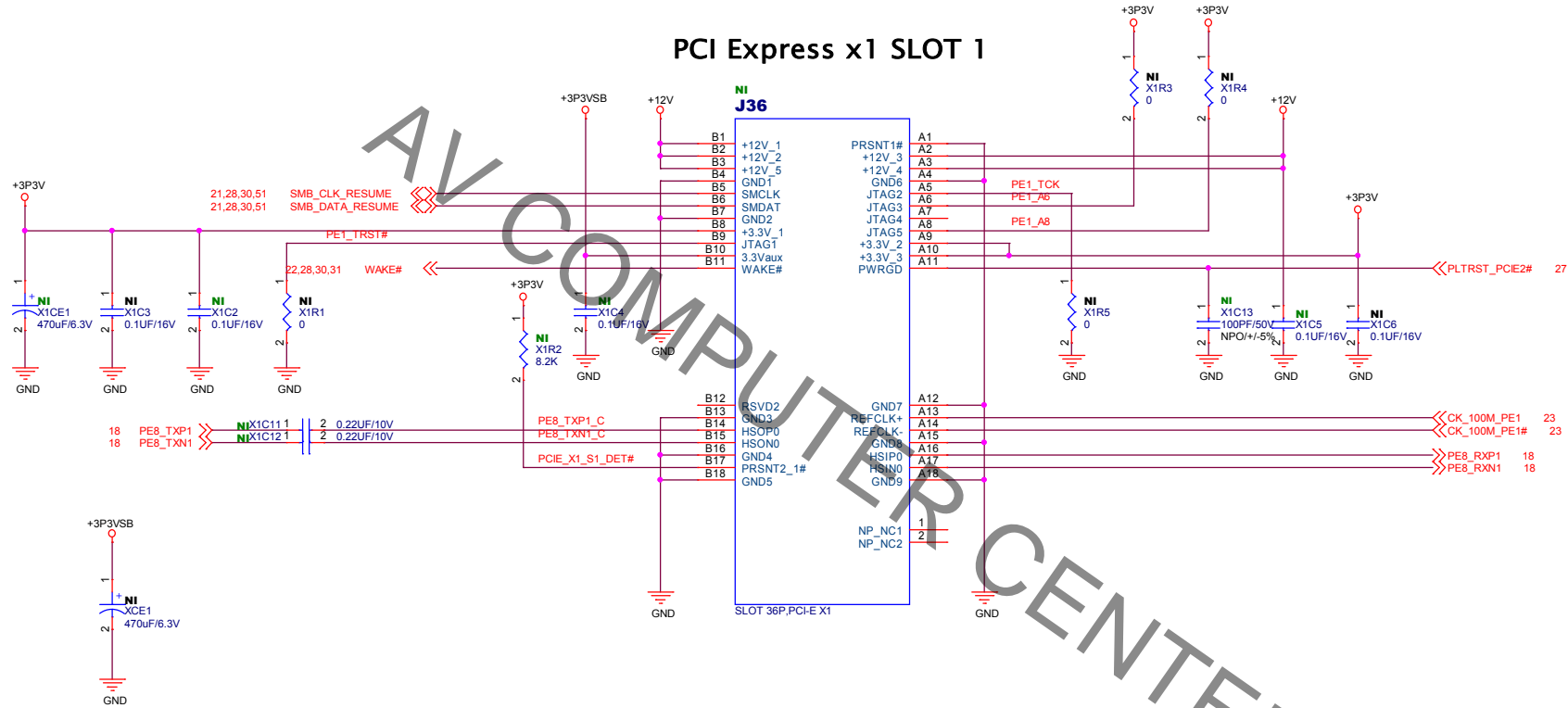




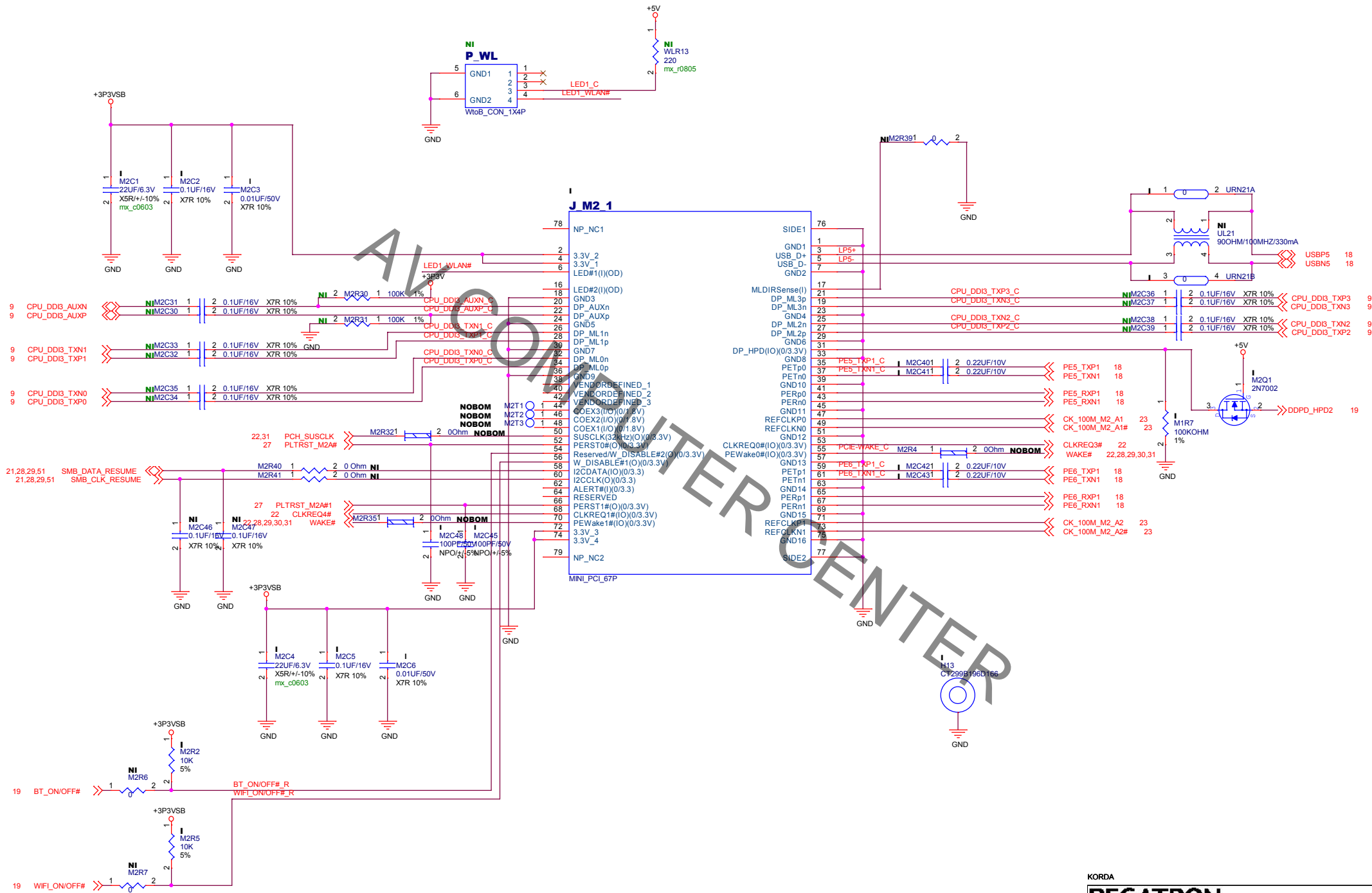
PCI EXPRESS X16 Graphics Card Slot

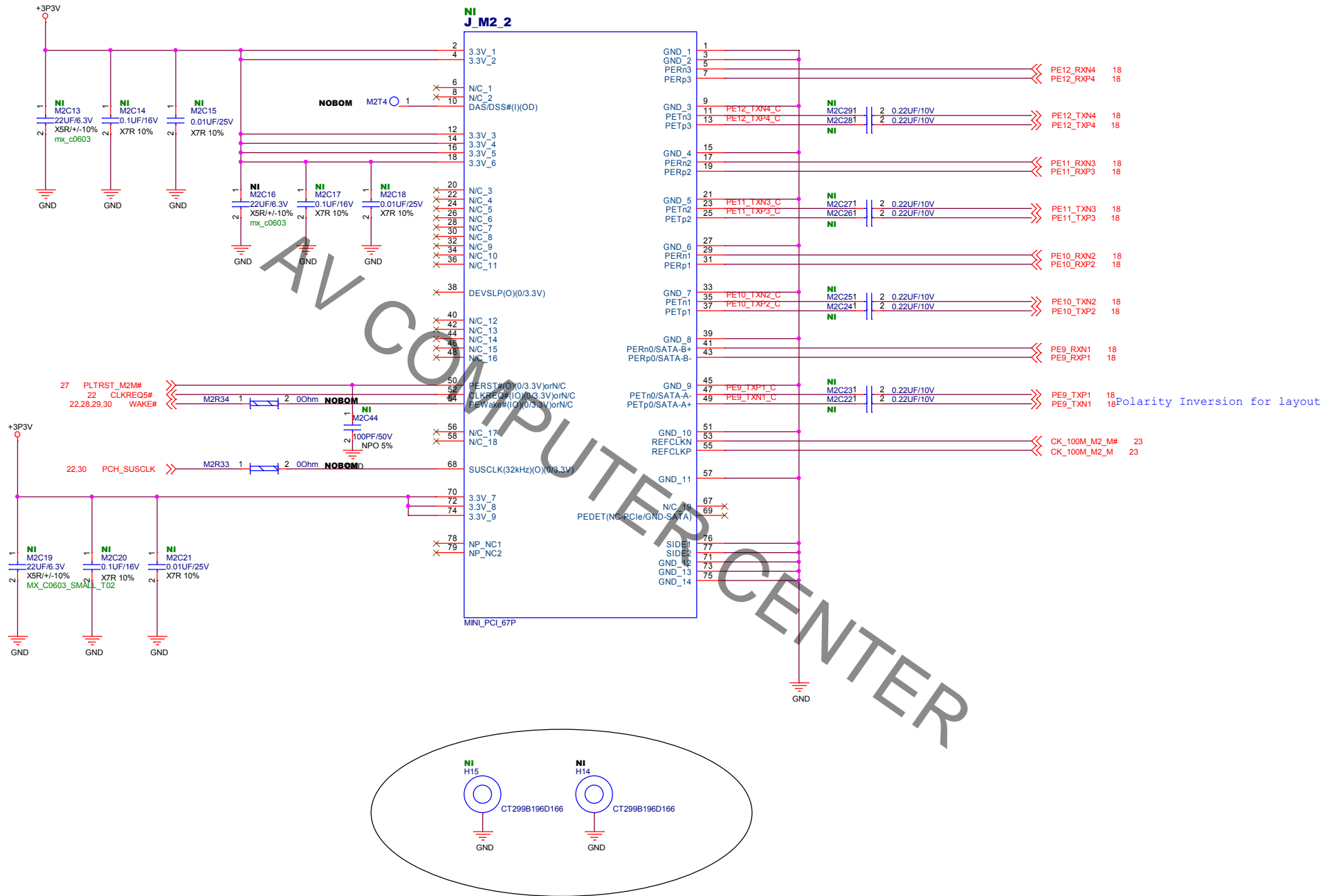


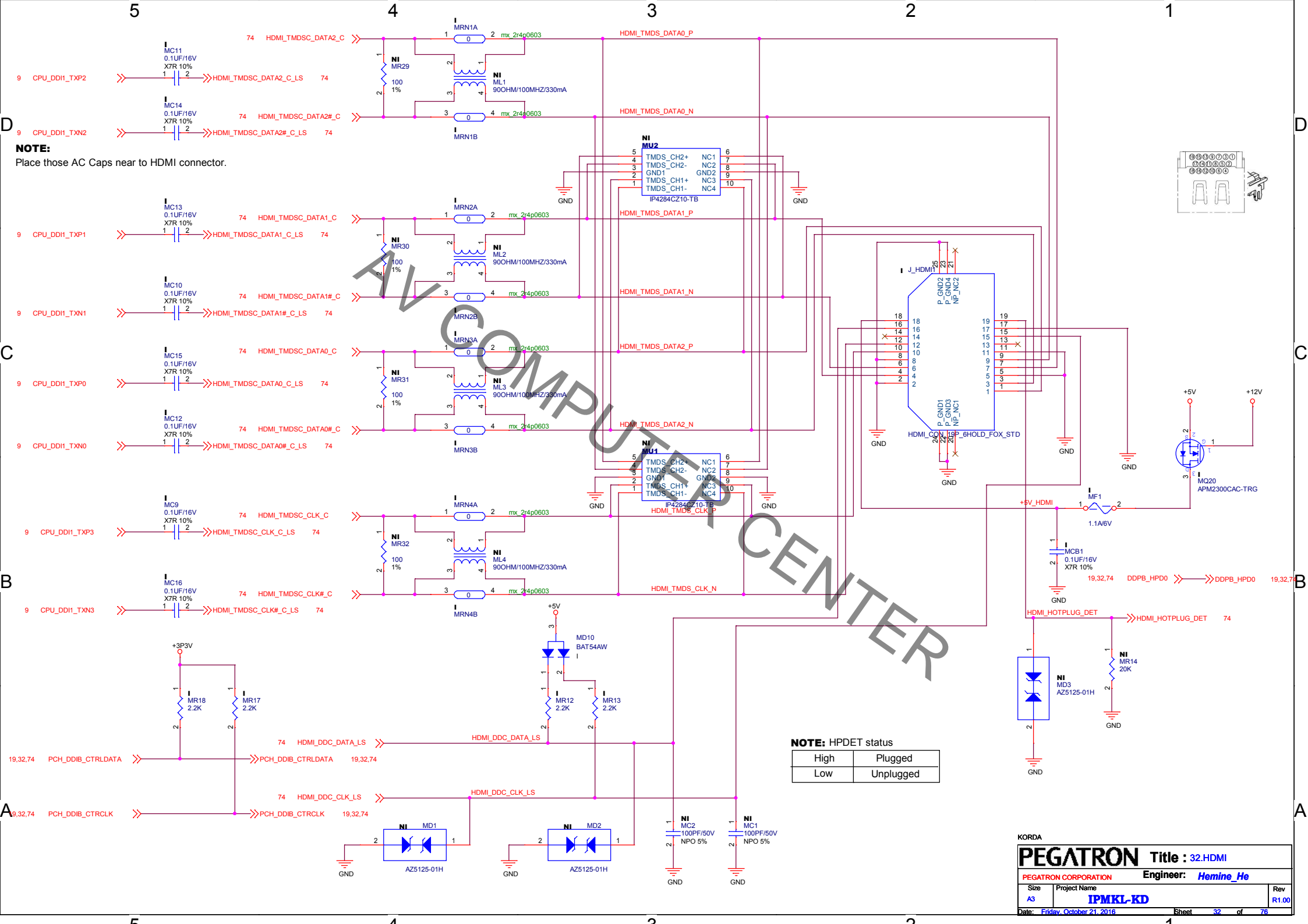
PCI Express x1 SLOT 1



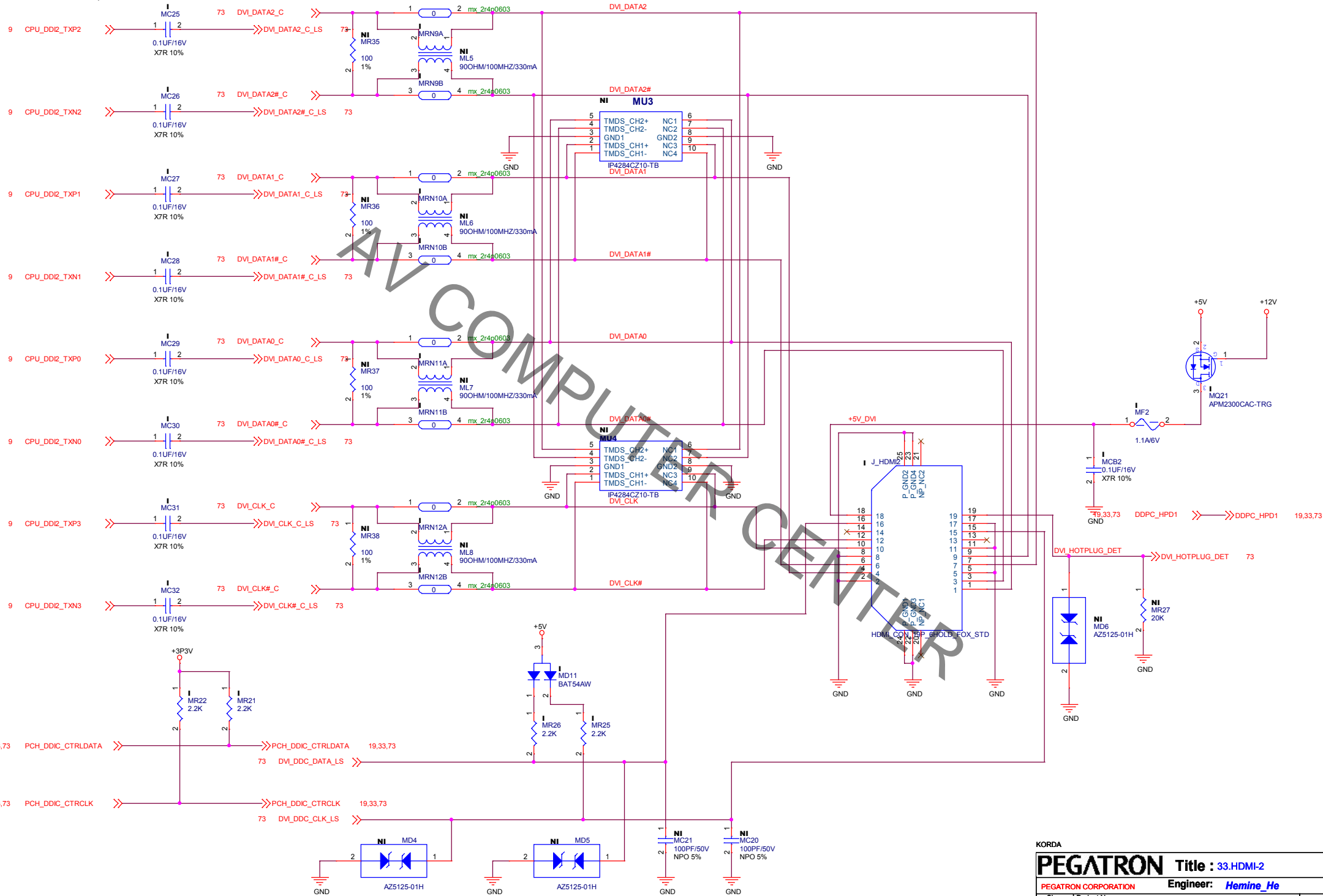
KORDA

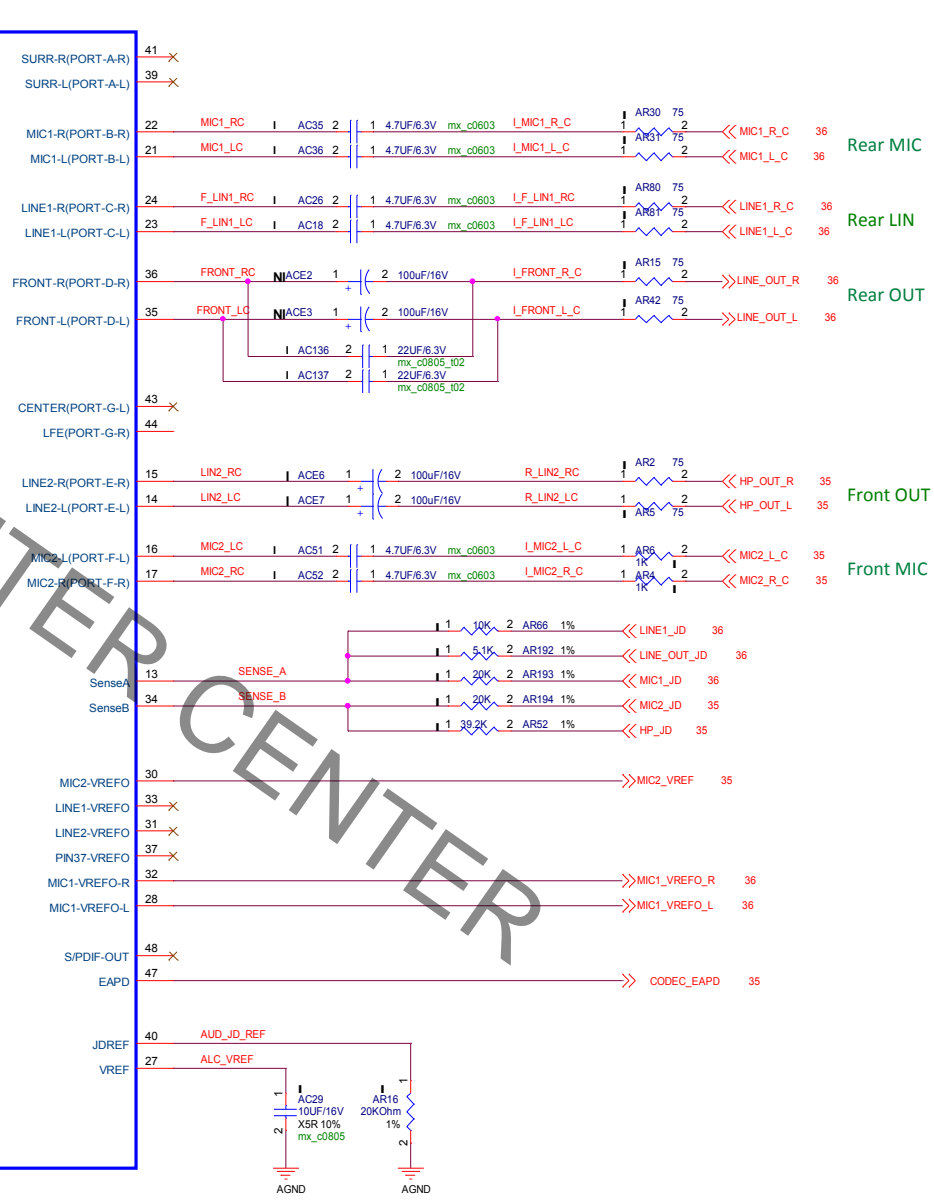
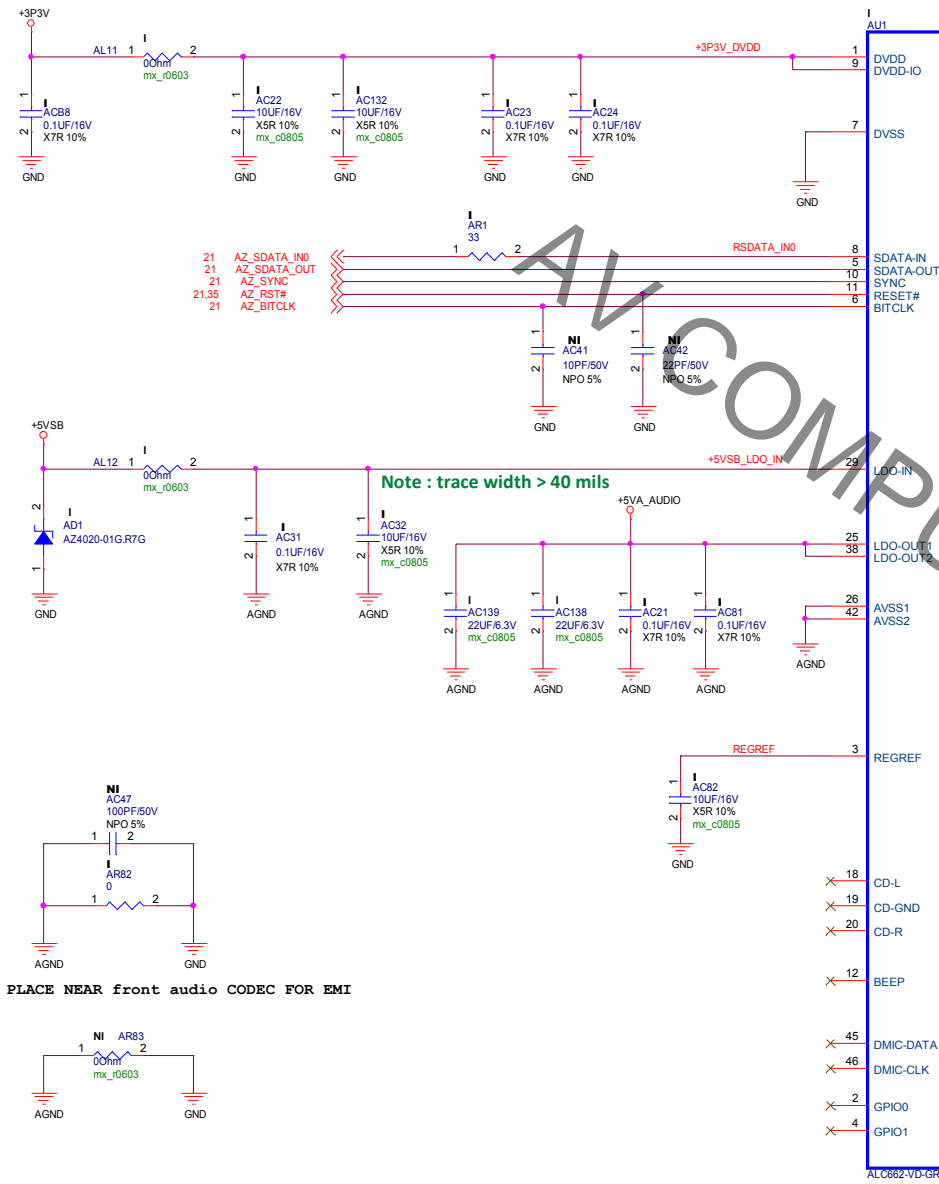


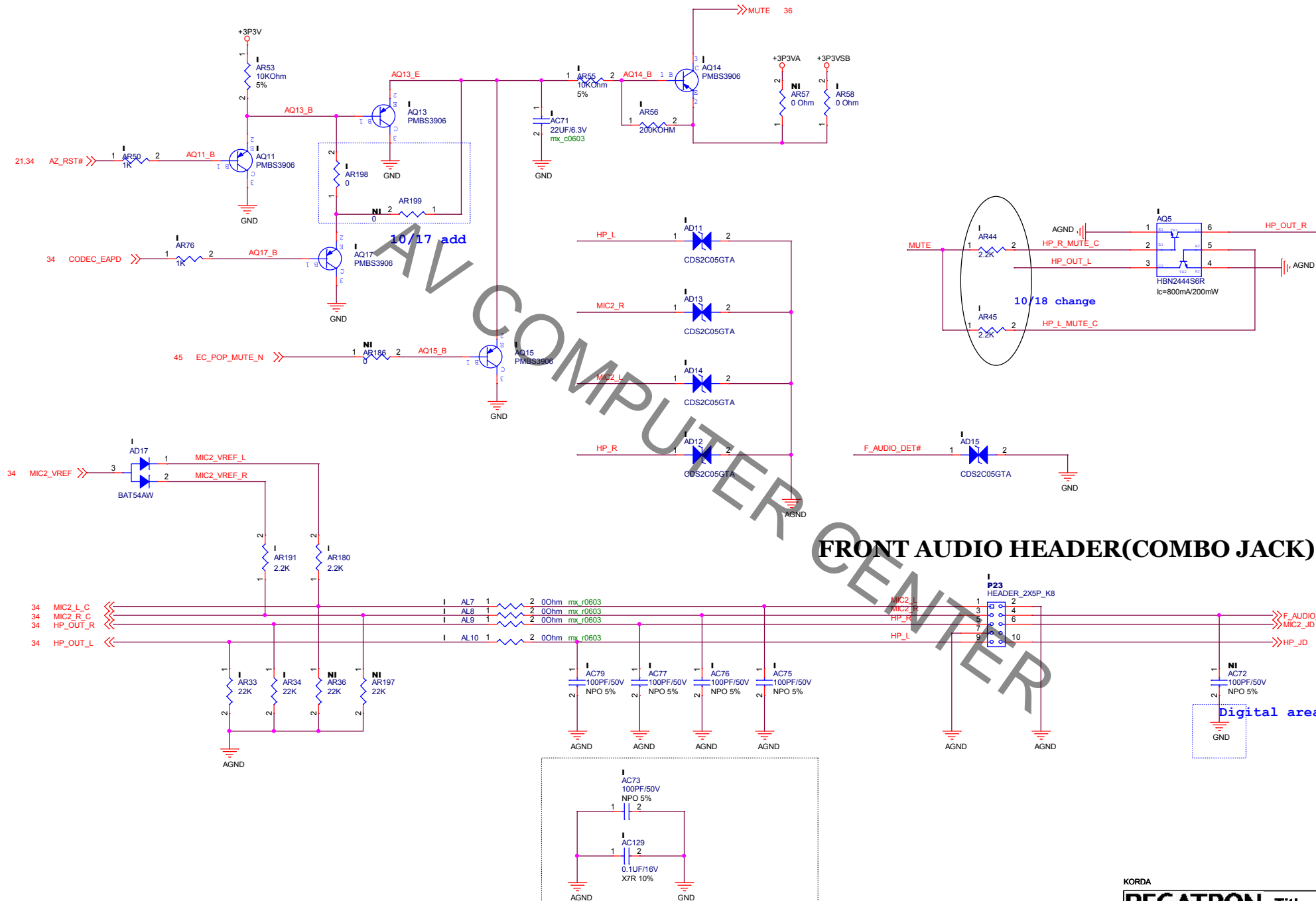




NOTE:
Place those AC Caps near to DVI connector.







FRONT AUDIO HEADER(COMBO JACK)

KORDA

PEGATRON Title : 35.FRONT AUDIO HEADER

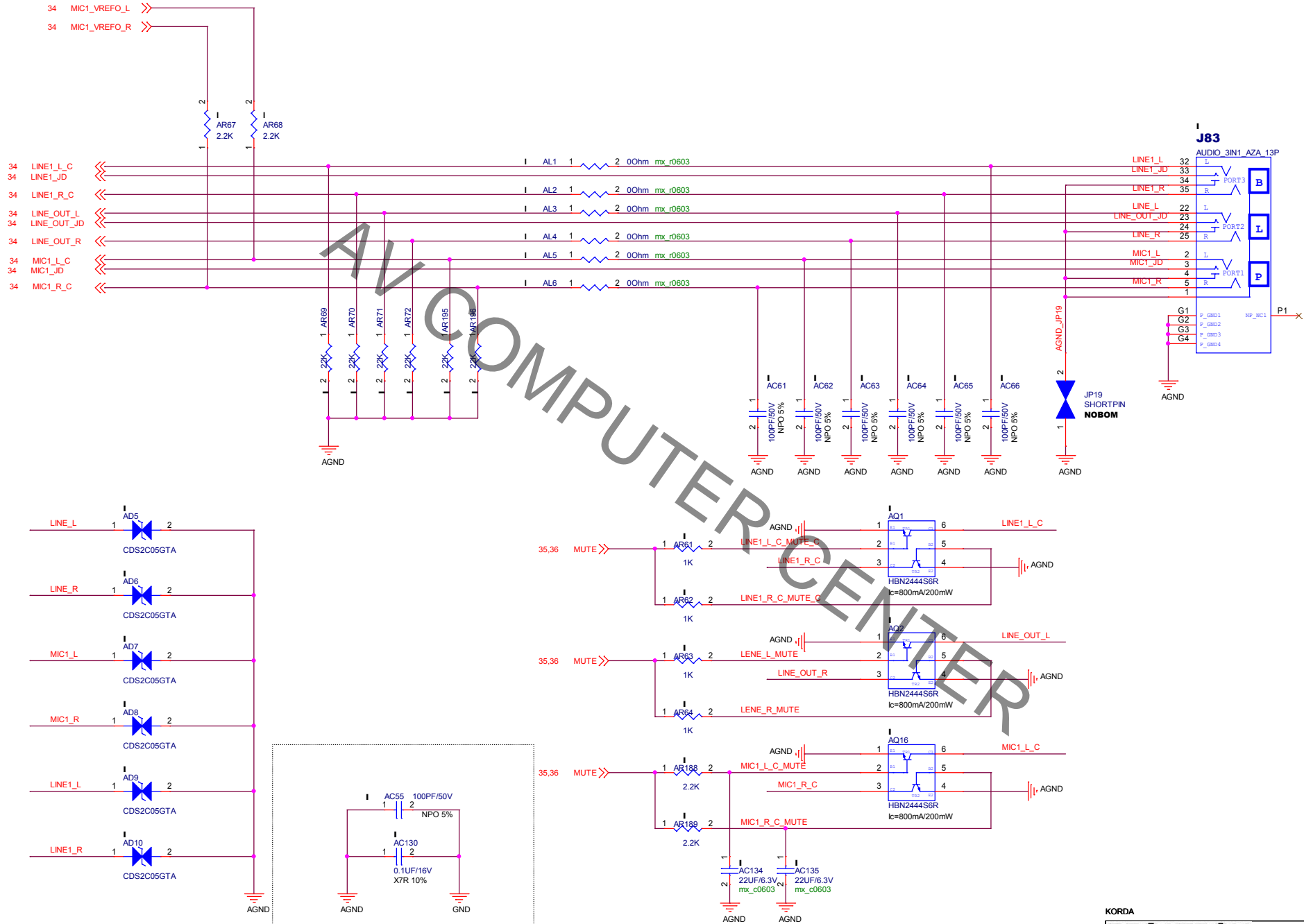
PEGATRON CORPORATION Engineer: Hemine_He

Size A3	Project Name IPMKL-KD	Rev R1.00
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Date: Friday, October 21, 2016

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AL87/AL89/AL91/AL93/AL95/AL97;Please use 09X131216000 instead of 0 ohm if you found have EMI issue



KORDA

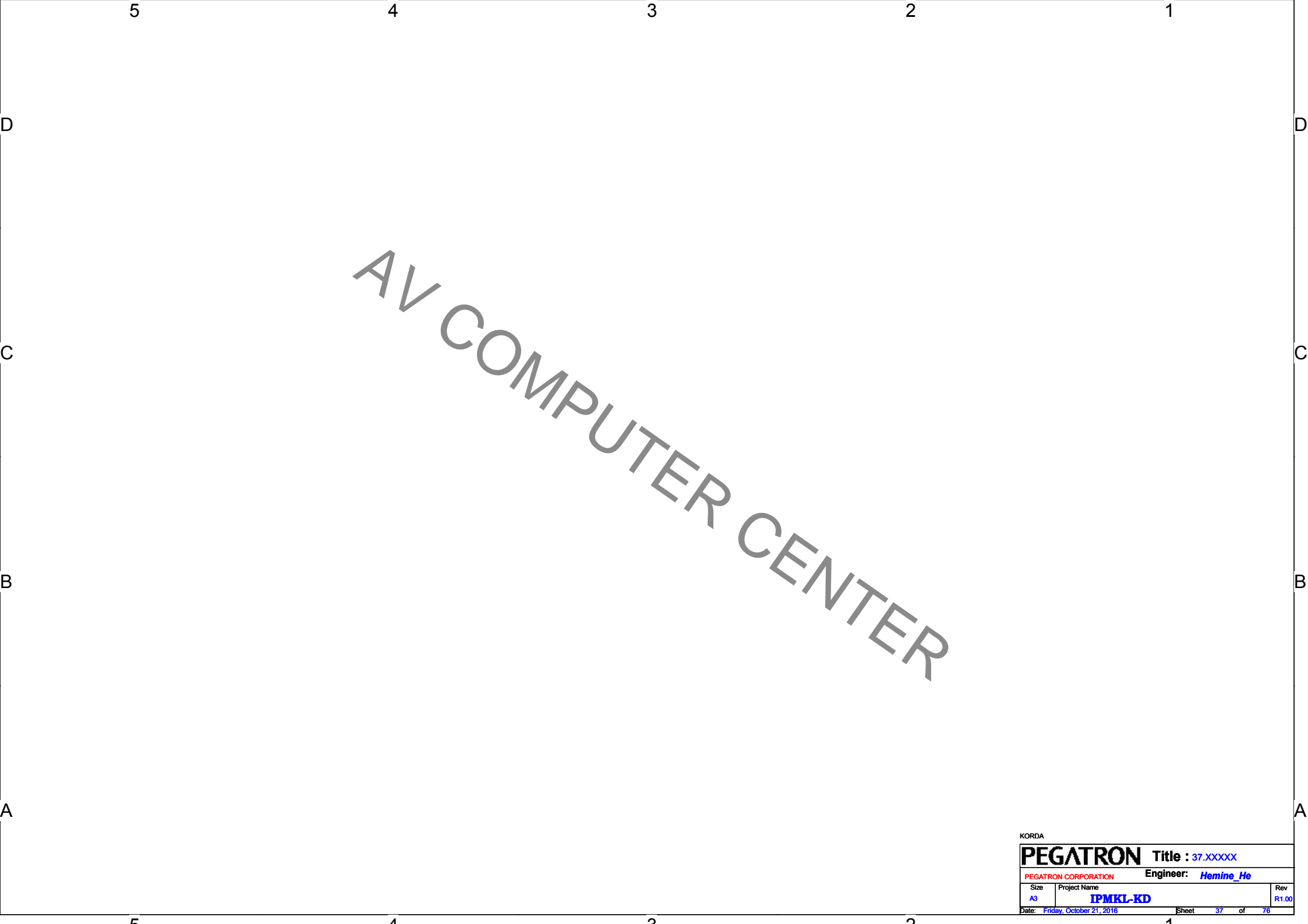
PEGATRON Title : 36.REAR AUDIO CONNECT

PEGATRON CORPORATION Engineer: *Hemine_He*

Size A3	Project Name IPMKL-KD	Rev R1.00
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Date: Friday, October 21, 2016	Sheet 36 of 76
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A horizontal number line is shown with a vertical tick mark at the center labeled $\frac{1}{2}$. The segment from 0 to $\frac{1}{2}$ is shaded blue, and the segment from $\frac{1}{2}$ to 1 is shaded red.



D

D

C

C

B

B

A

A

5

4

3

2

1

5

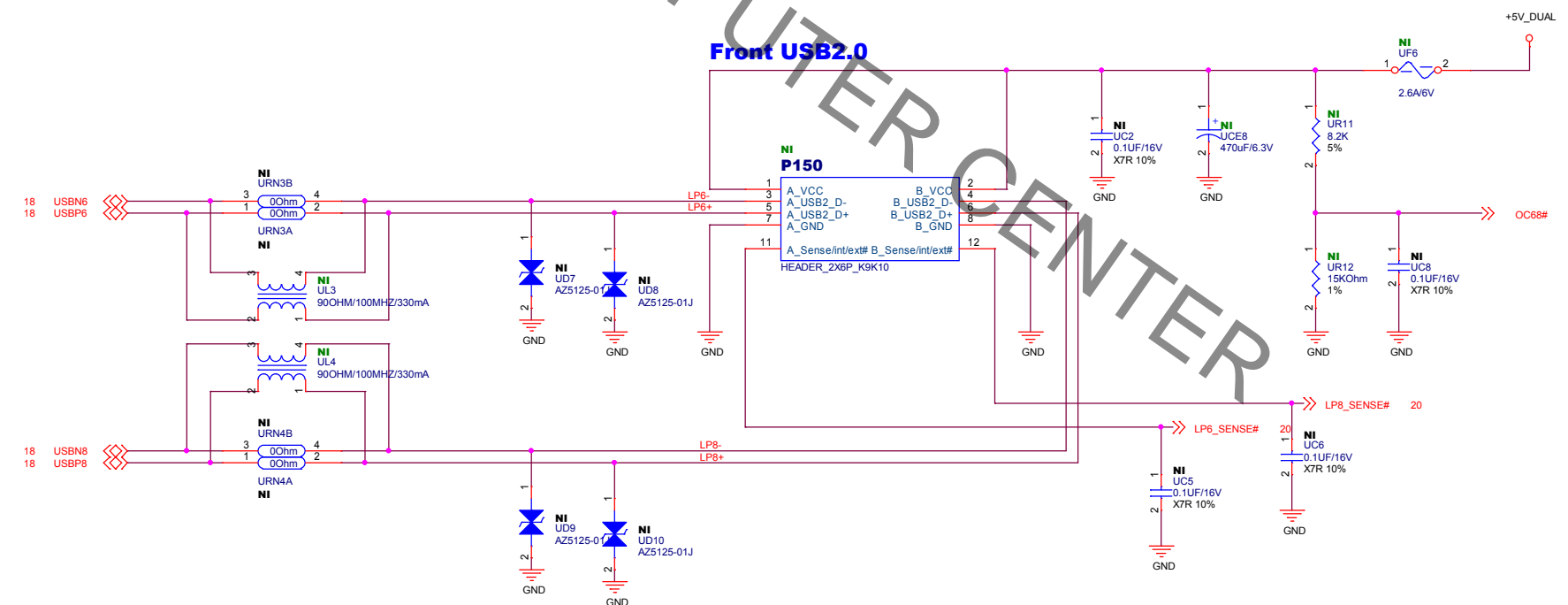
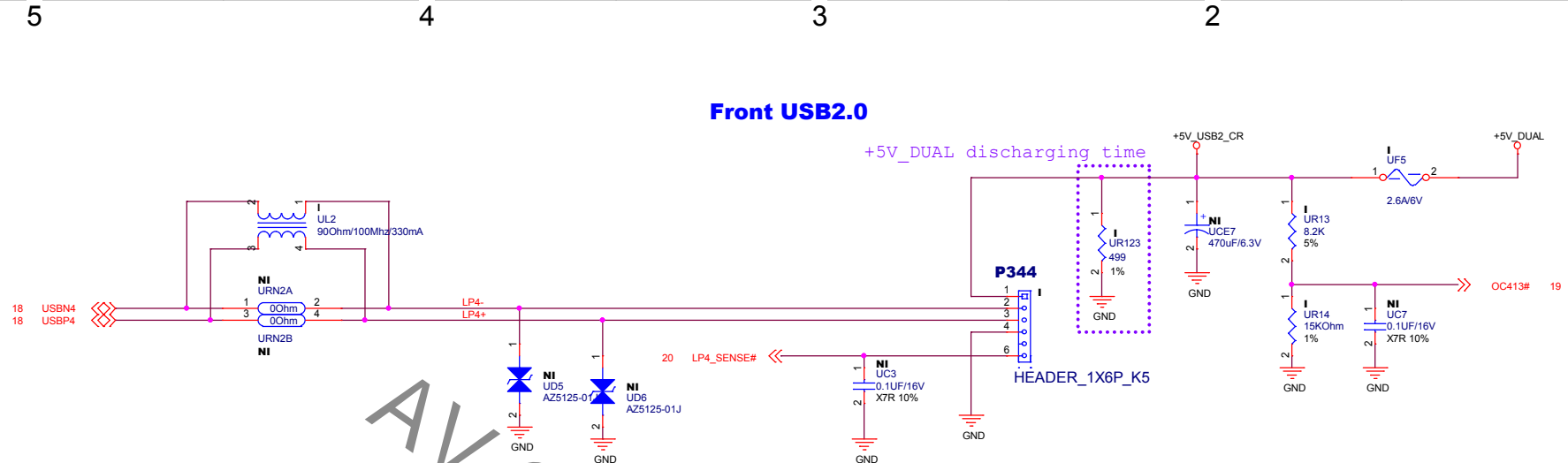
4

3

2

1

KORDA		
PEGATRON		Title : 37.XXXXX
PEGATRON CORPORATION		Engineer: Hemine_He
Size A3	Project Name IPMKL-KD	Rev R1.00
Date: Friday, October 21, 2016		
Sheet 37 of 76		

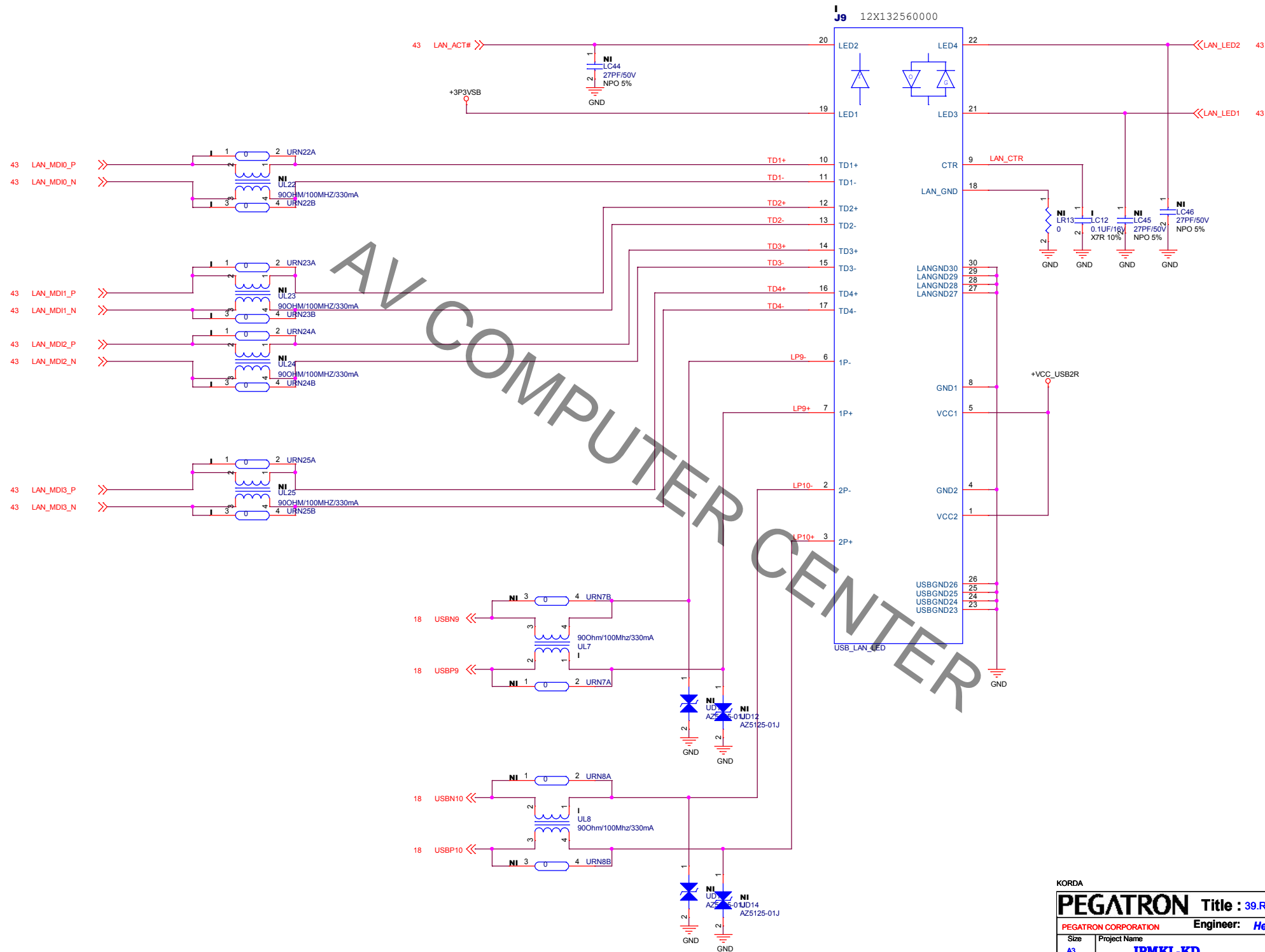


D

C

B

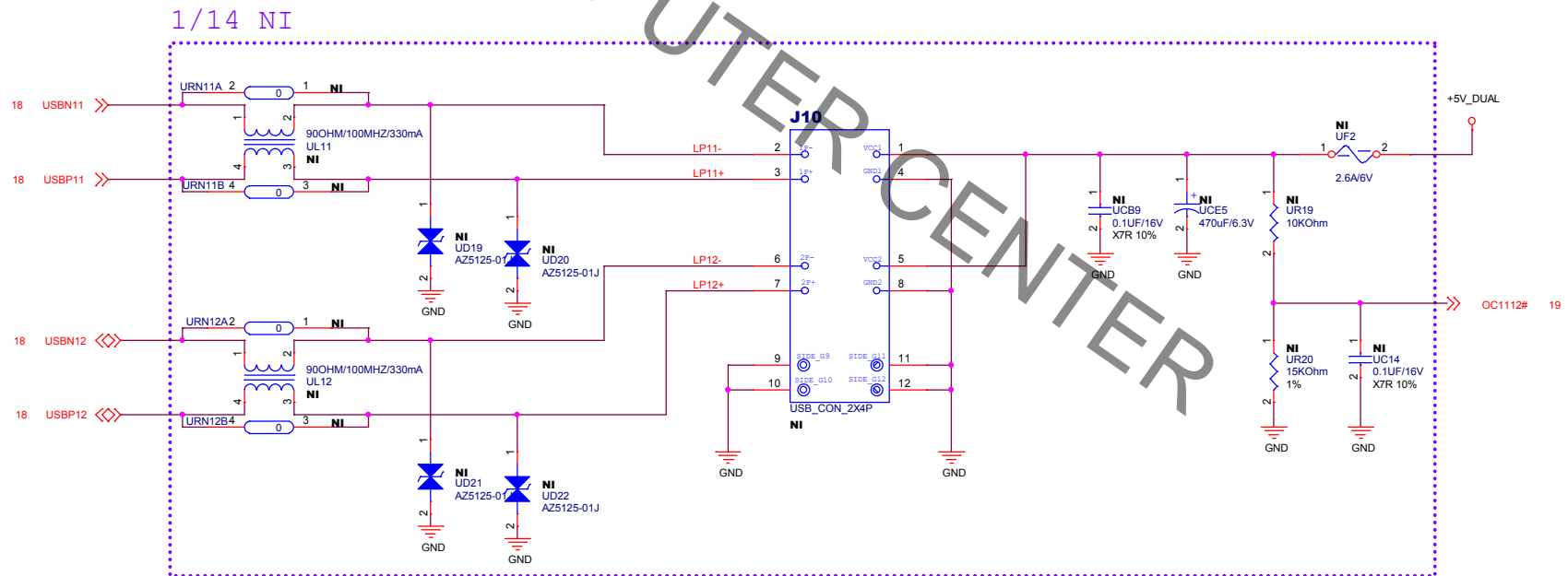
A



KORDA

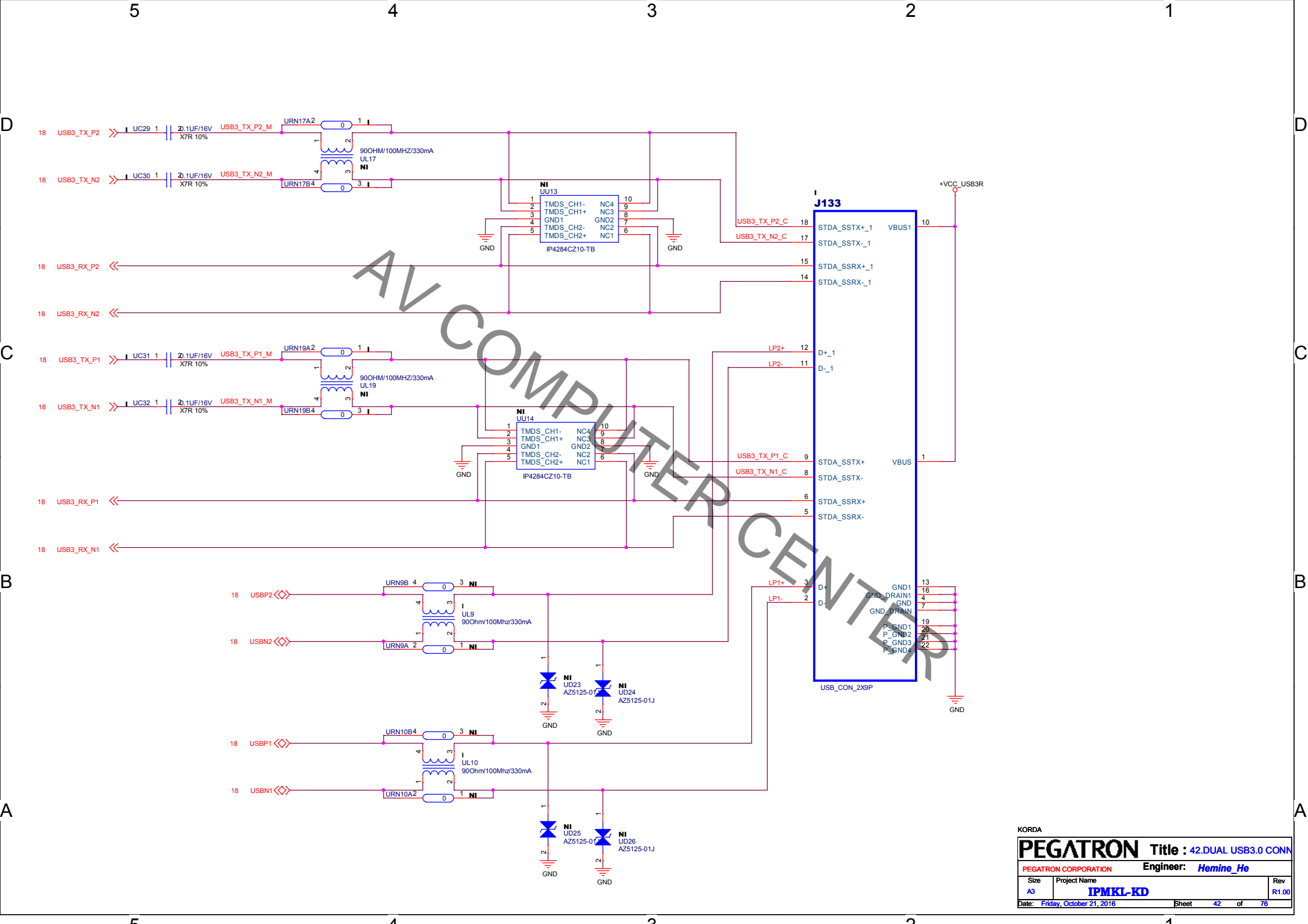
PEGATRON		Title : 39.RJ45+USB2.0 CONN	
PEGATRON CORPORATION		Engineer: <u>Hemine_He</u>	
Size A3	Project Name IPMKL-KD		Rev R1.00
Date: <u>Friday, October 21, 2016</u>		Sheet	39 of 76

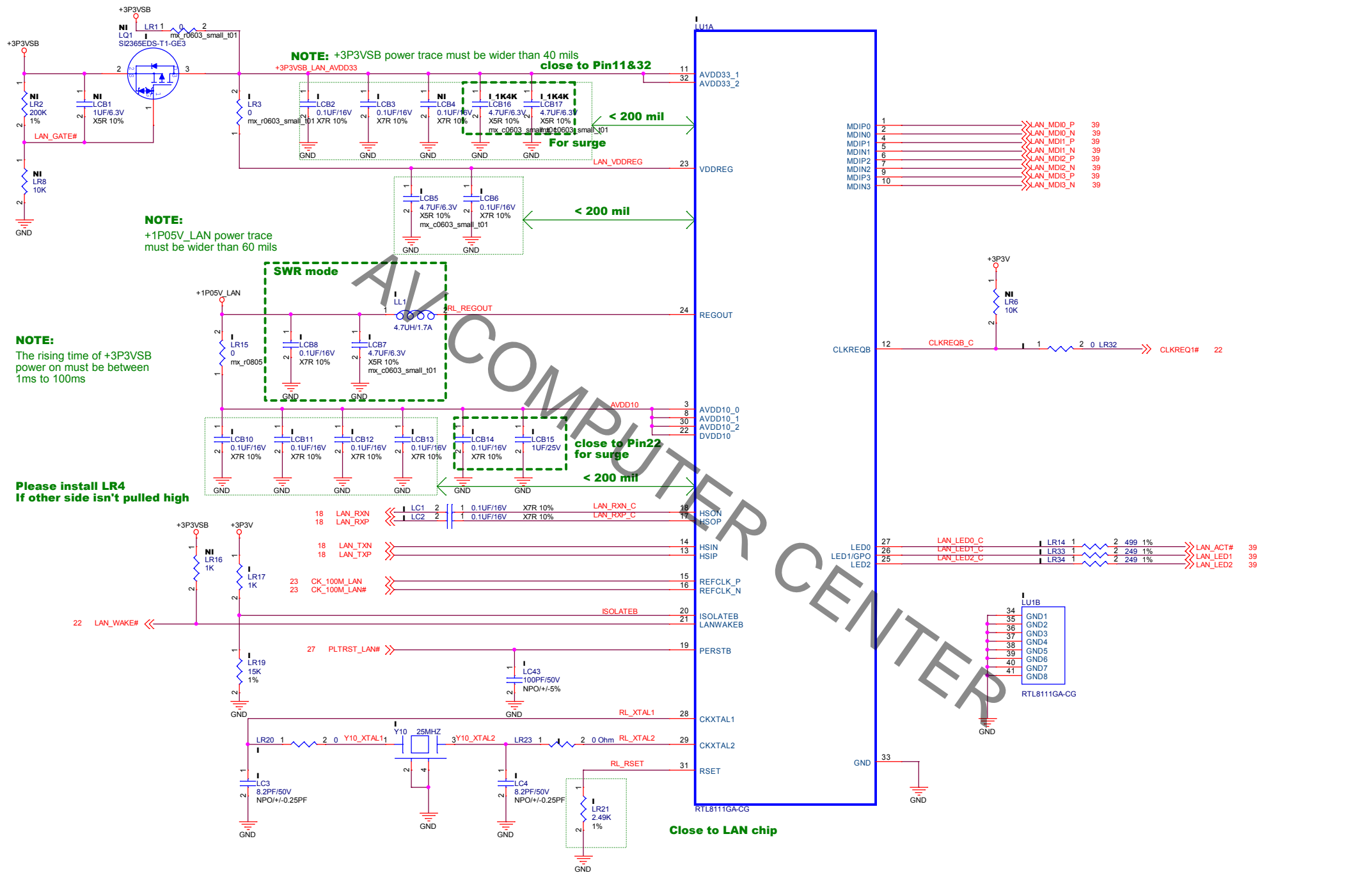
AV COMPUTER CENTER

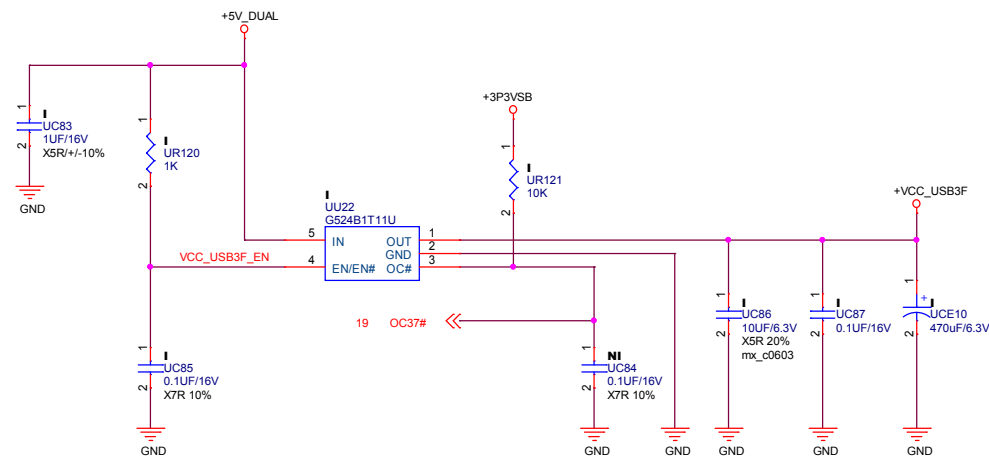
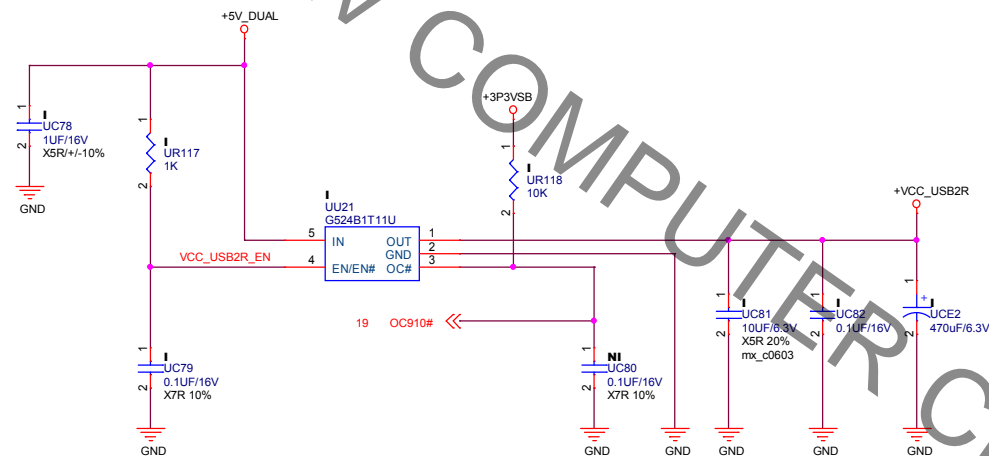
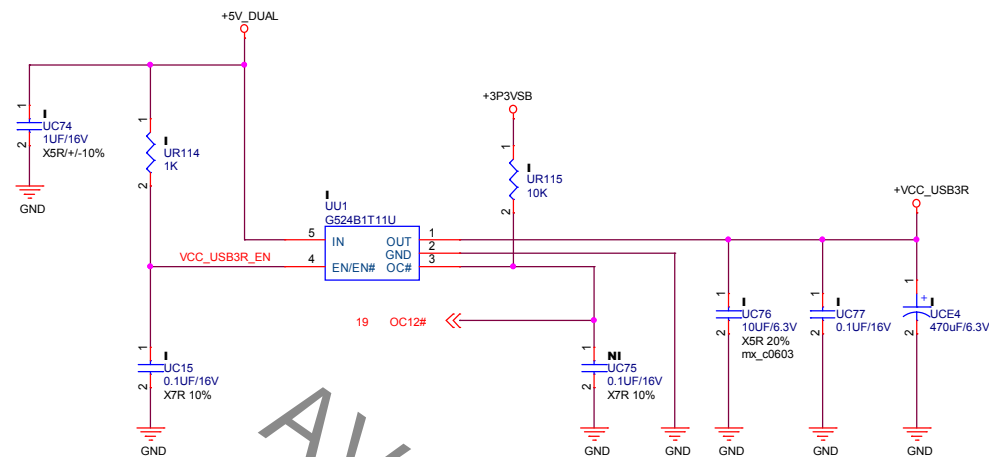


KORDA

PEGATRON		Title : 41.DUAL USB2.0 CONN-NI	
PEGATRON CORPORATION		Engineer: <i>Hemine_He</i>	
Size A3	Project Name IPMKL-KD		Rev R1.00
Date: <i>Friday, October 21, 2016</i>		Sheet 41 of 76	

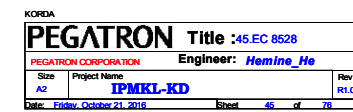


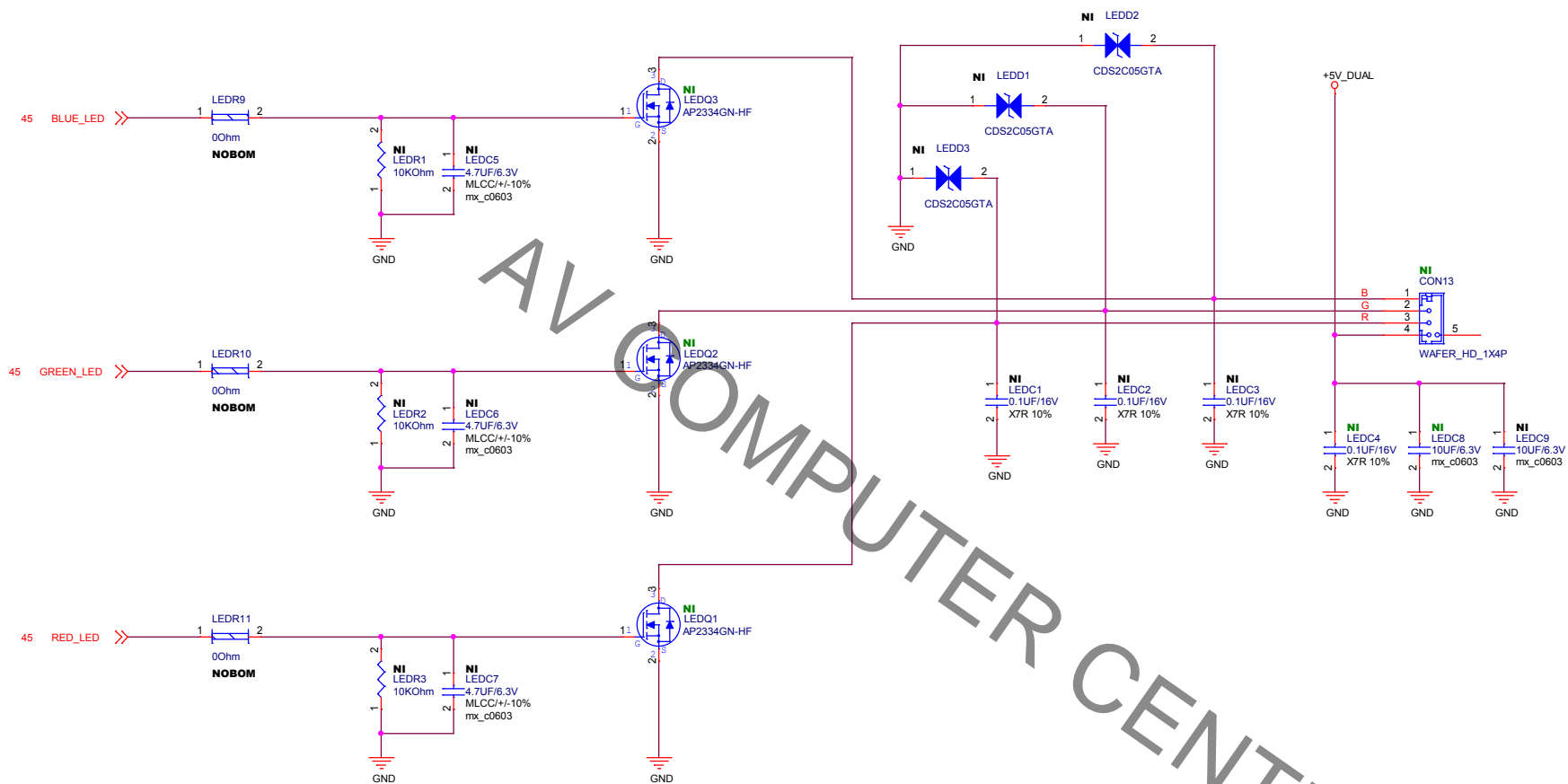




KORDA

PEGATRON		Title : 44.USB POWER	
PEGATRON CORPORATION		Engineer: <u>Hemine_He</u>	
Size A3	Project Name IPMKL-KD	Rev R1.00	
Date: Friday, October 21, 2016		Sheet	44 of 76

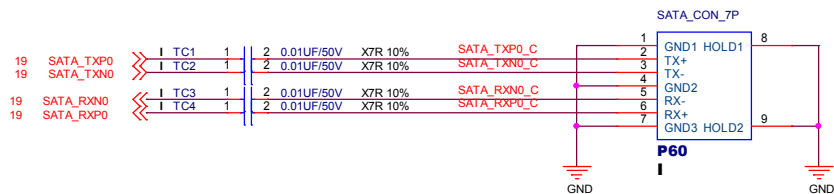




KORDA

PEGATRON		Title : 46.CHASSIS LED Light	
PEGATRON CORPORATION		Engineer: <u>Hemine_He</u>	
Size	Project Name	Rev	
A3	IPMKL-KD	R1.00	
Date: <u>Friday, October 21, 2016</u>		Sheet <u>46</u> of <u>76</u>	

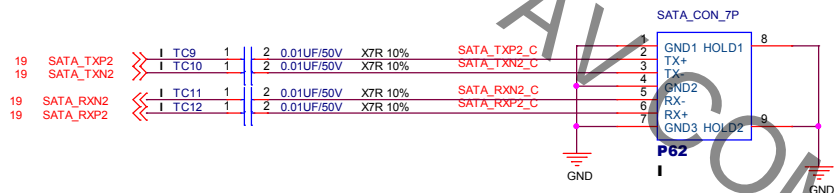
HDD Connector
COLOR = Dark BLUE



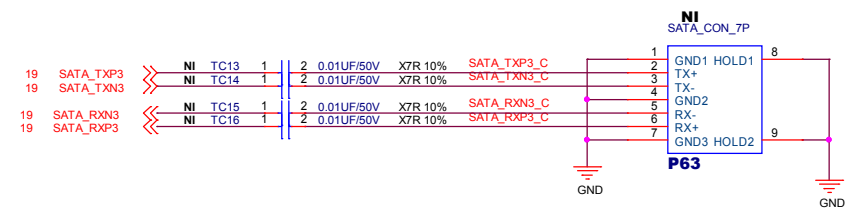
COLOR=ORANGE

1/26 Removed.

COLOR=WHITE



COLOR=LIGHT BLUE

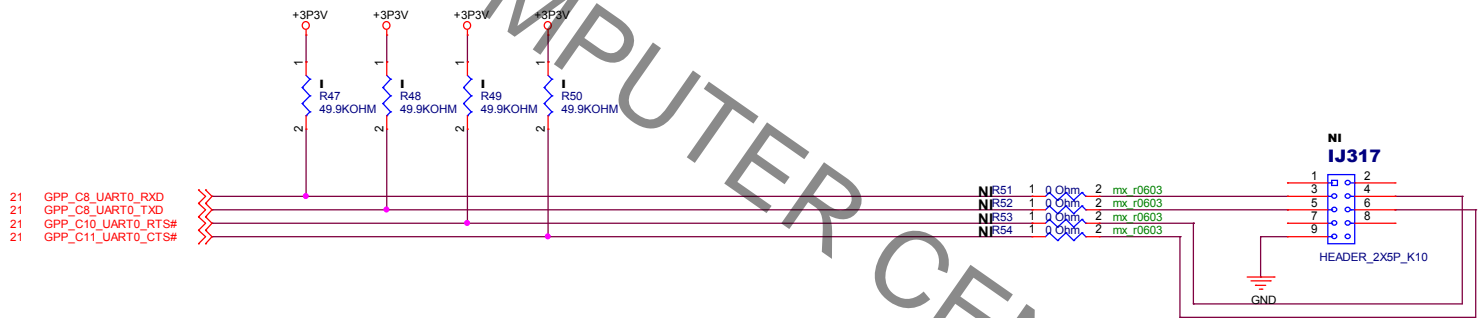


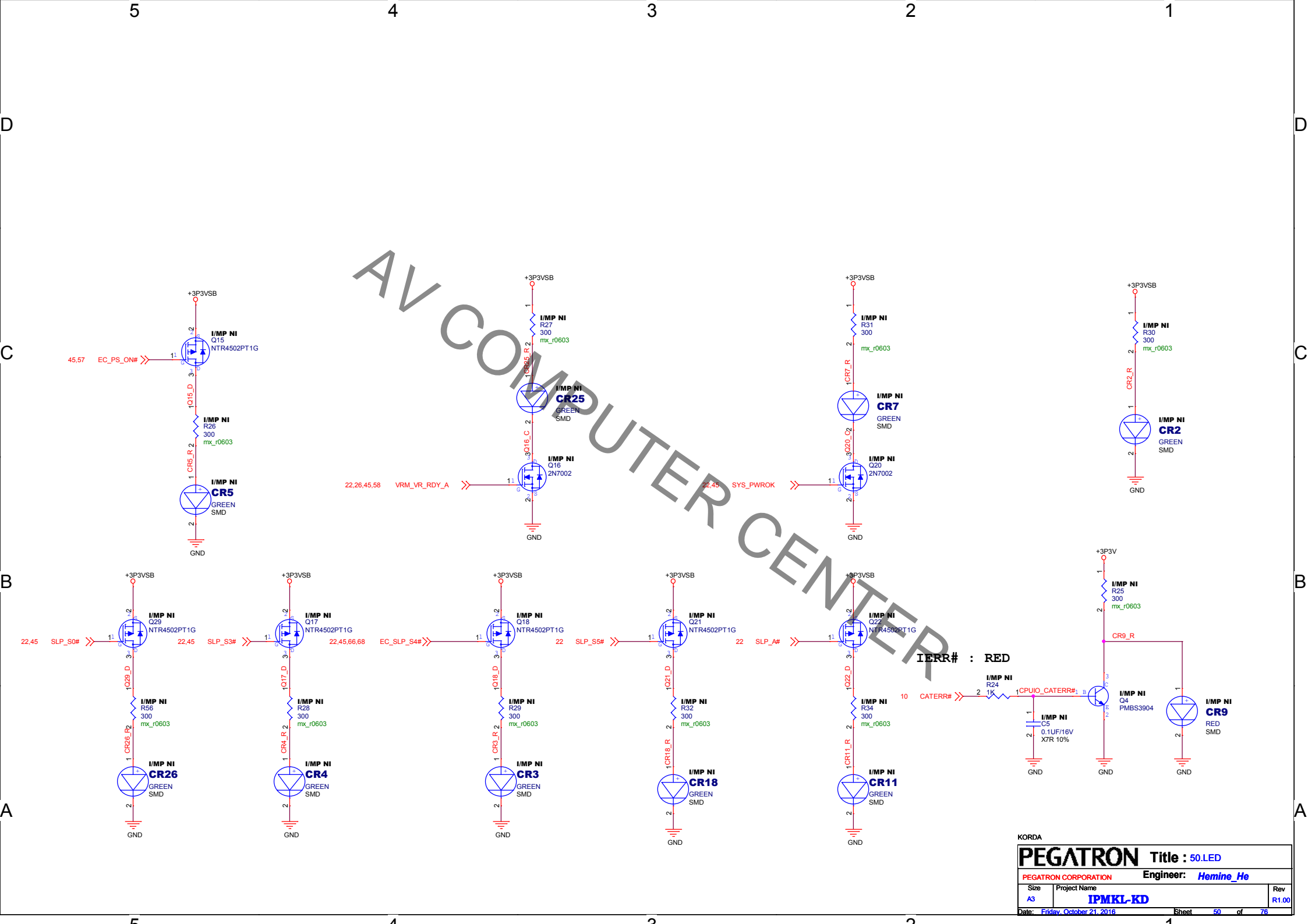
COLOR=RED

1/26 Removed.

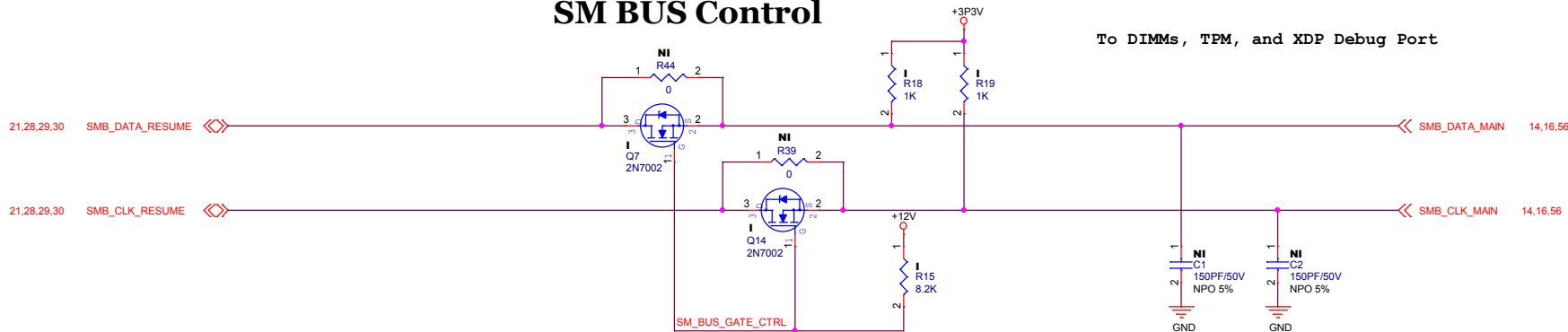
AV COMPUTER CENTER

Reserve for WIN7 WHQL Debug Port

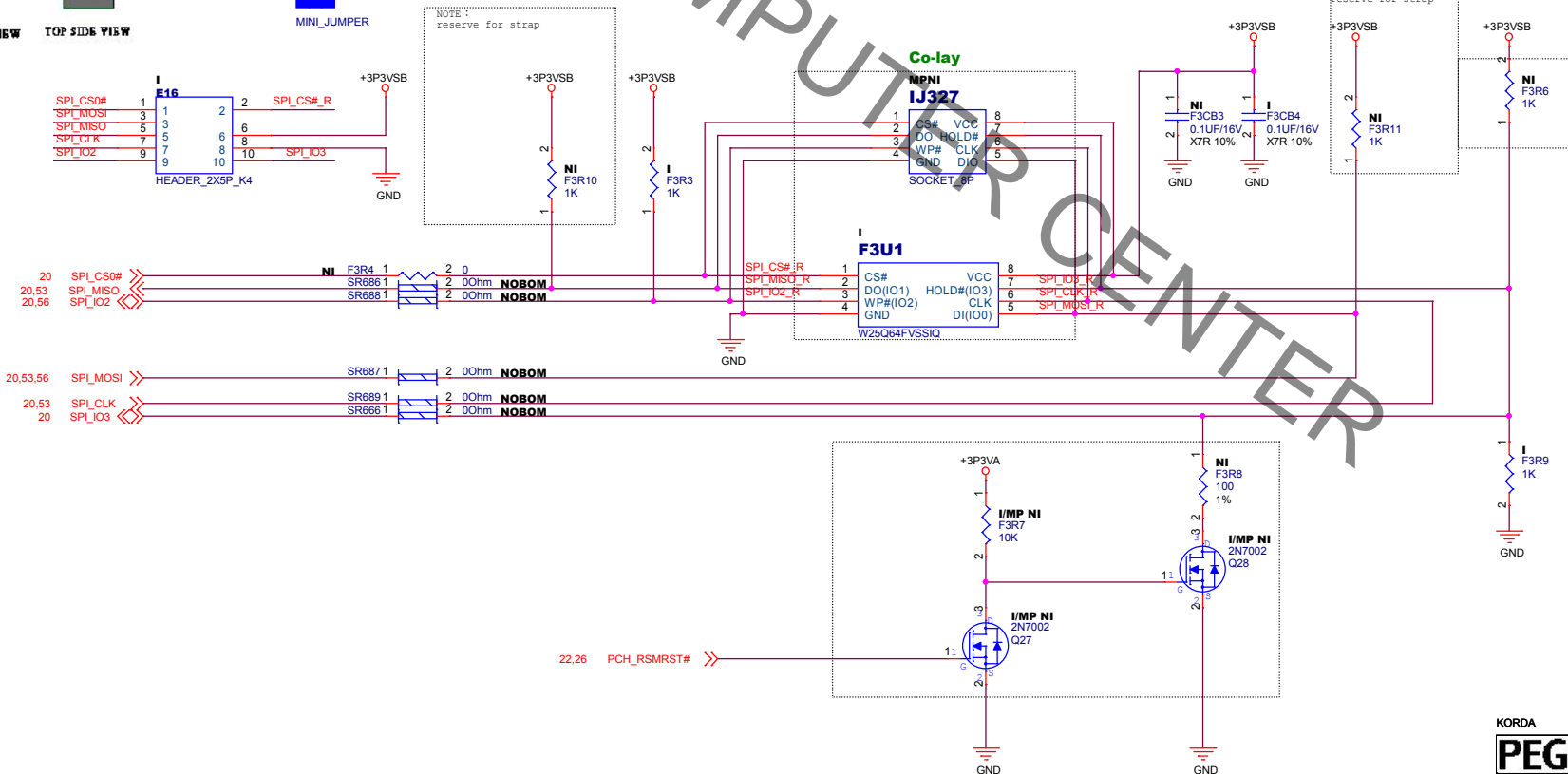
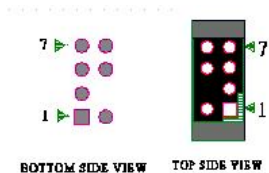




SM BUS Control

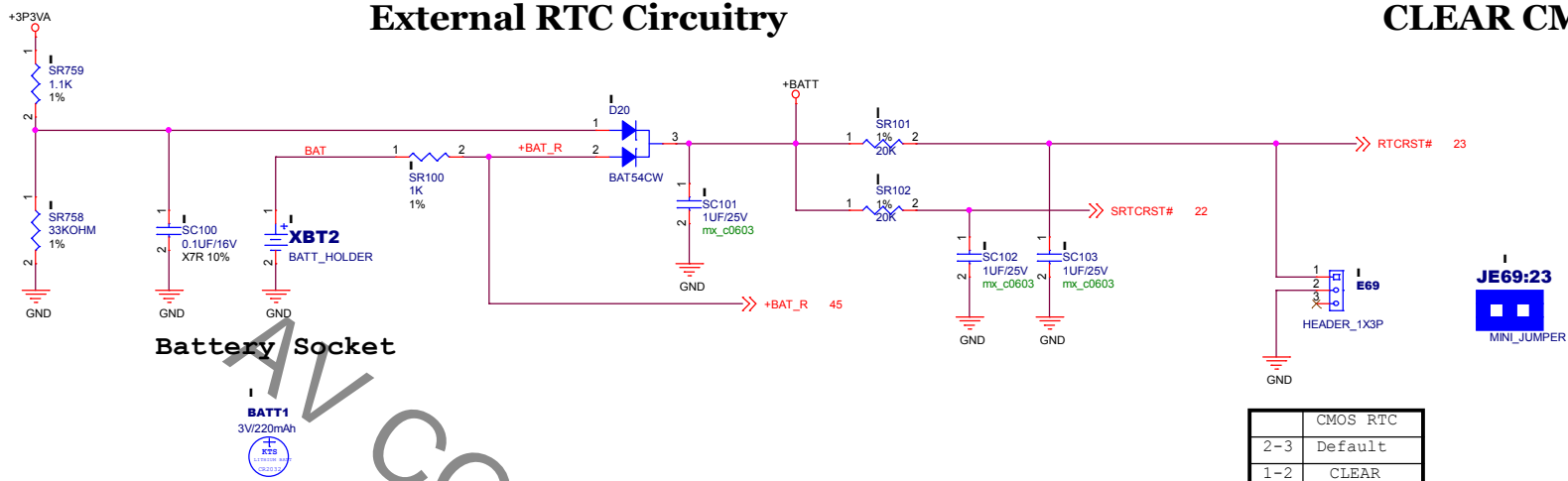


SPI BIOS ROM - 128Mbit

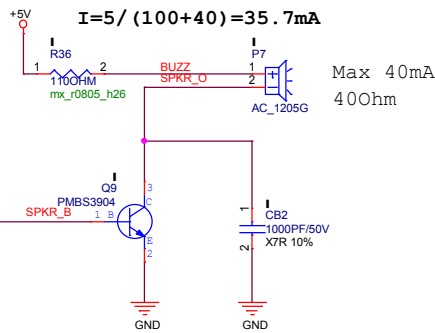


External RTC Circuitry

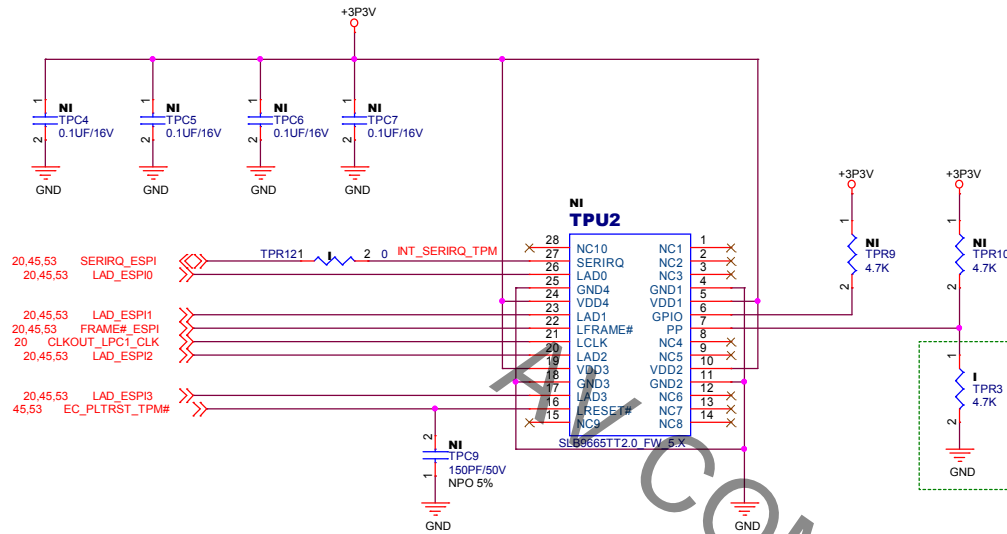
CLEAR CMOS



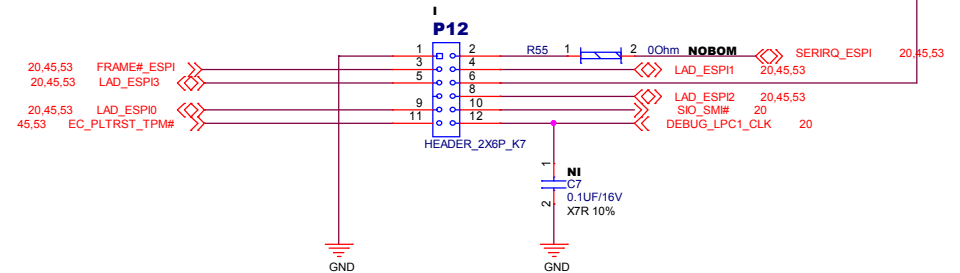
SPEAKER



TPM1

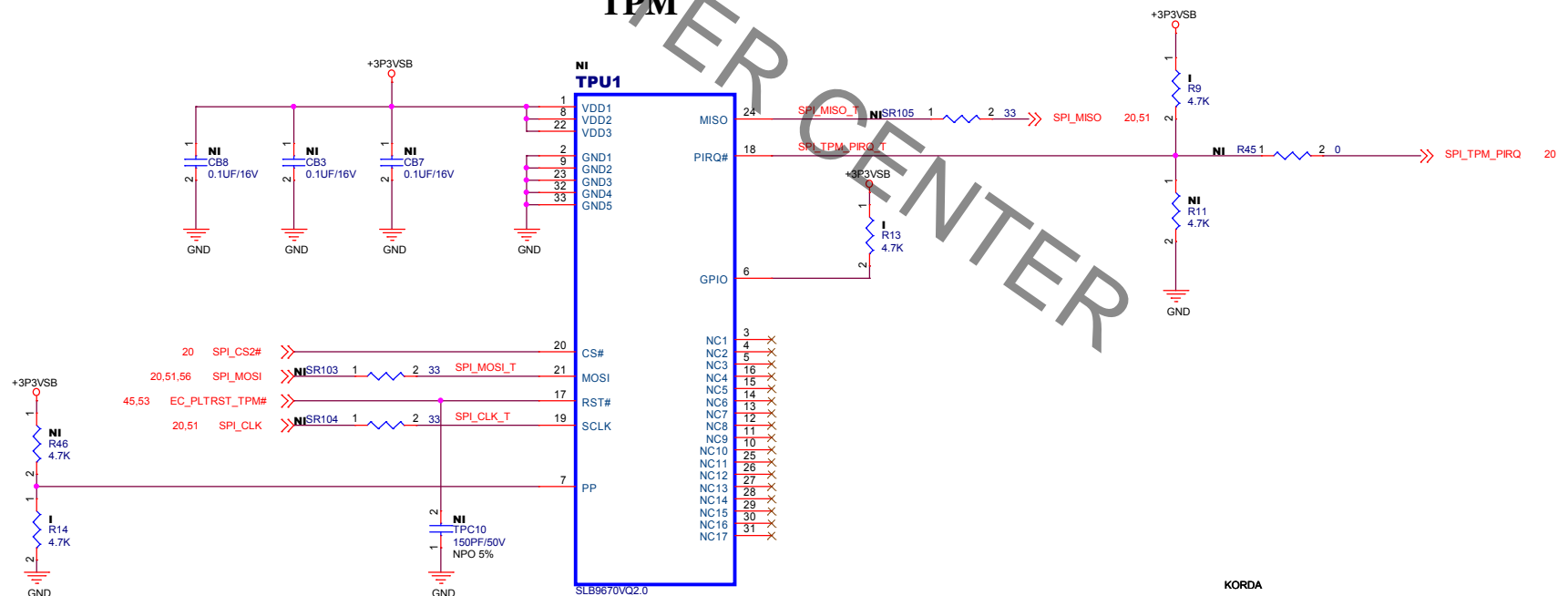


LPC DEBUG1



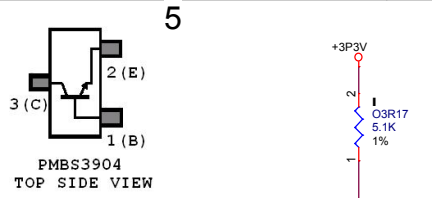
TPM2.0 pull low

TPM



KORDA

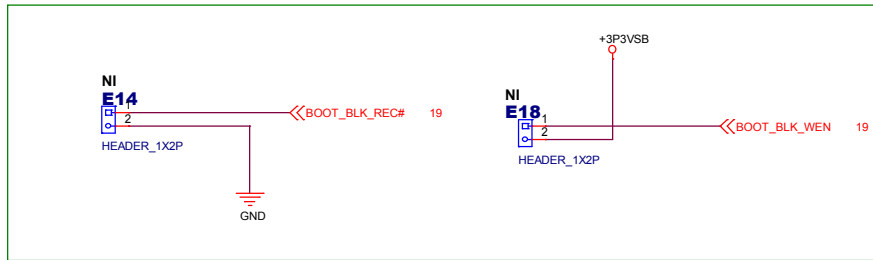
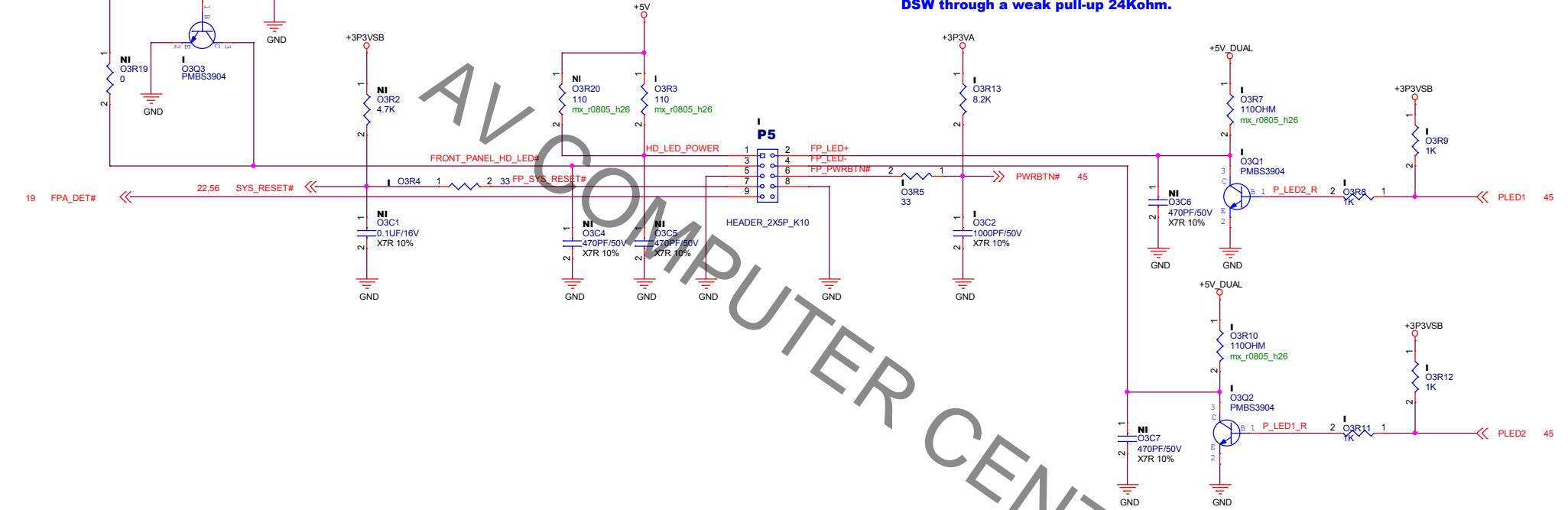
PEGATRON			Title : 53.TPM/LPC Debug Header	
PEGATRON CORPORATION			Engineer: <u>Hemine_He</u>	
Size	Project Name		Rev	
A3	IPMKL-KD		R1.00	
Date: Friday, October 21, 2016		Sheet	53	of 76



FRONT PANEL / LED CIRCUITRY

NOTE:

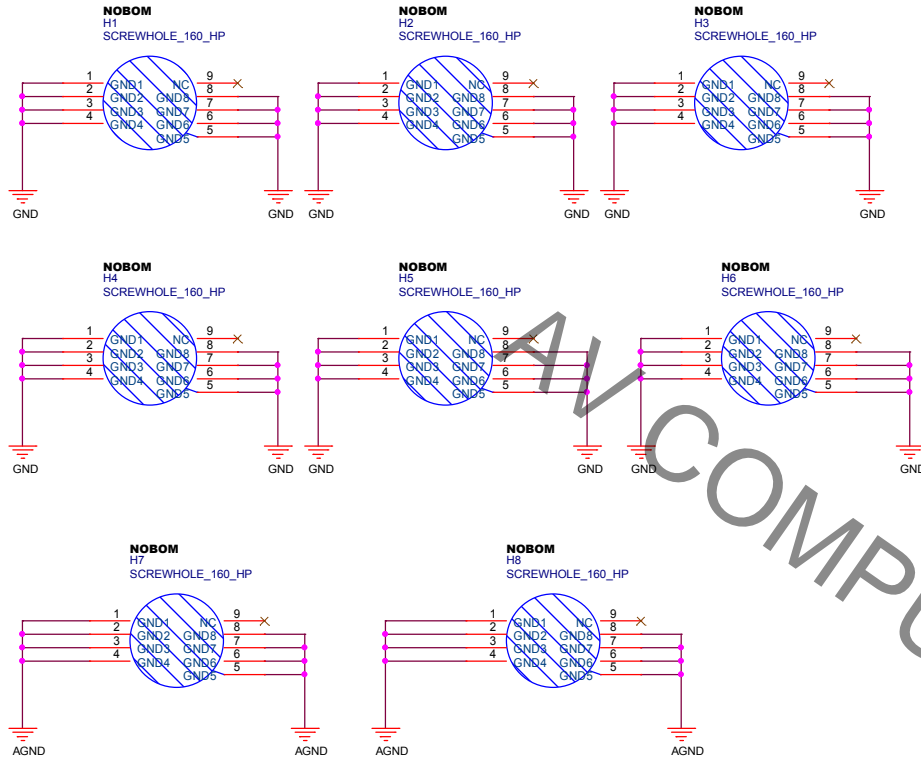
PWRBTN# of PCH is internally pulled-up in PCH to 3.3 V DSW through a weak pull-up 24Kohm.



KORDA

PEGATRON		Title : 54.FRONT PANEL	
PEGATRON CORPORATION		Engineer: <i>Hemine_He</i>	
Size A3	Project Name IPMKL-KD	Rev R1.00	
Date: Friday, October 21, 2016		Sheet 54 of 76	

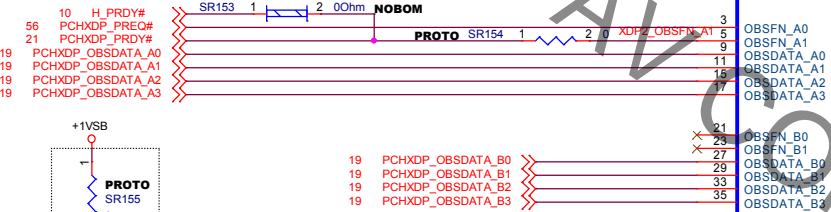
ONLY FOR INTEL SCREW HOLE



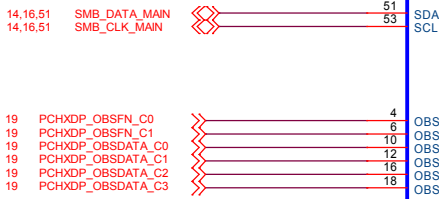
INTEL PCH XDP DEBUG PORT

NOTE:
Place strap resistors of TDO near to XDP connector,
and TDI and TMS near to CPU.

NOTE:
Check OBSFN_A[0:1] direction

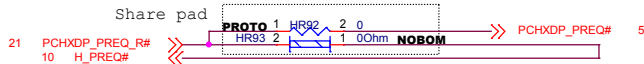


NOTE:
Connecting ITPCLK/HOOK4 is optional; can be left floated

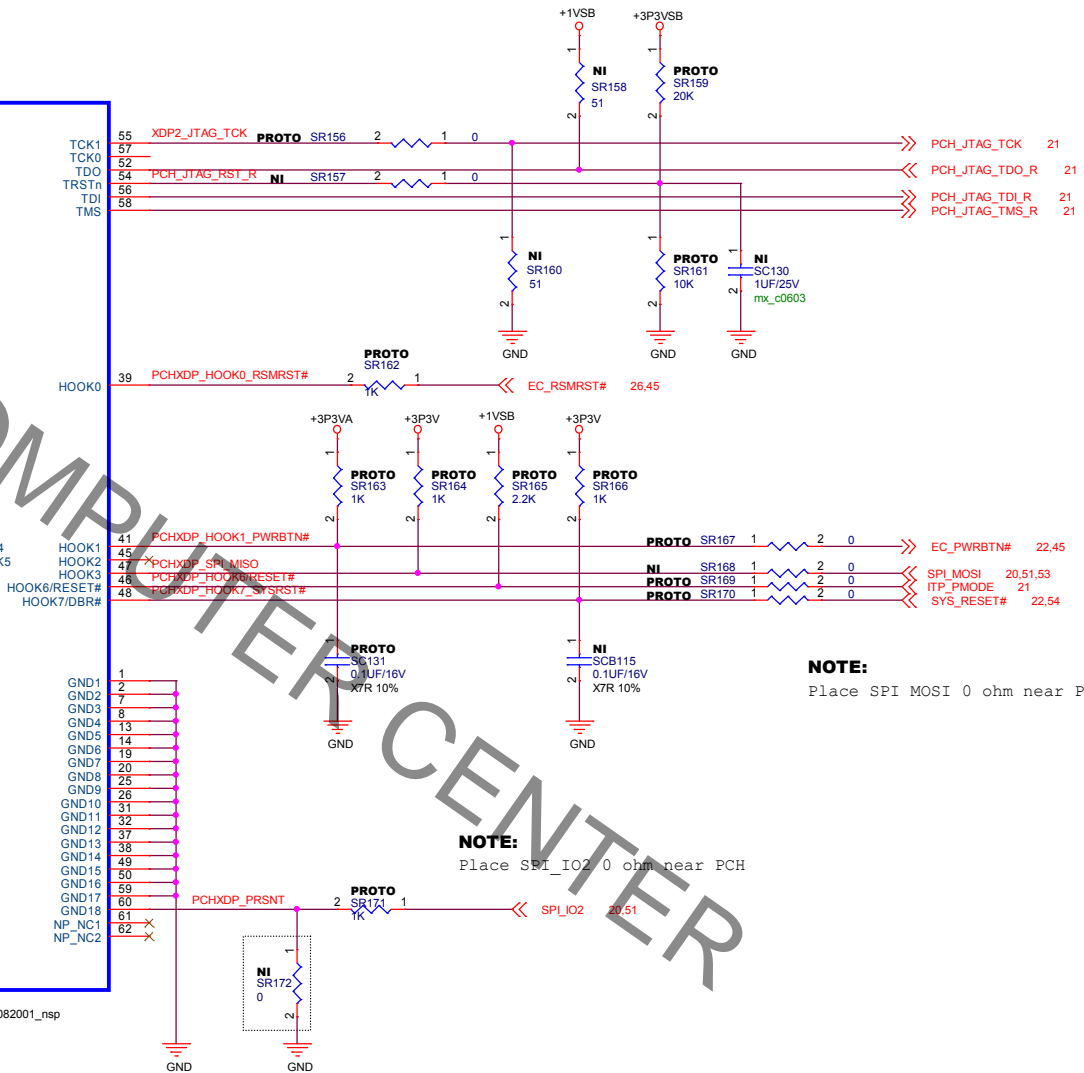


NOTE: PREQ# and PRDY#

MUST be routed in this order: Debug Port -> CPU -> PCH-H.



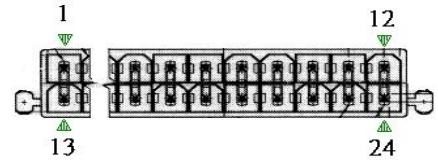
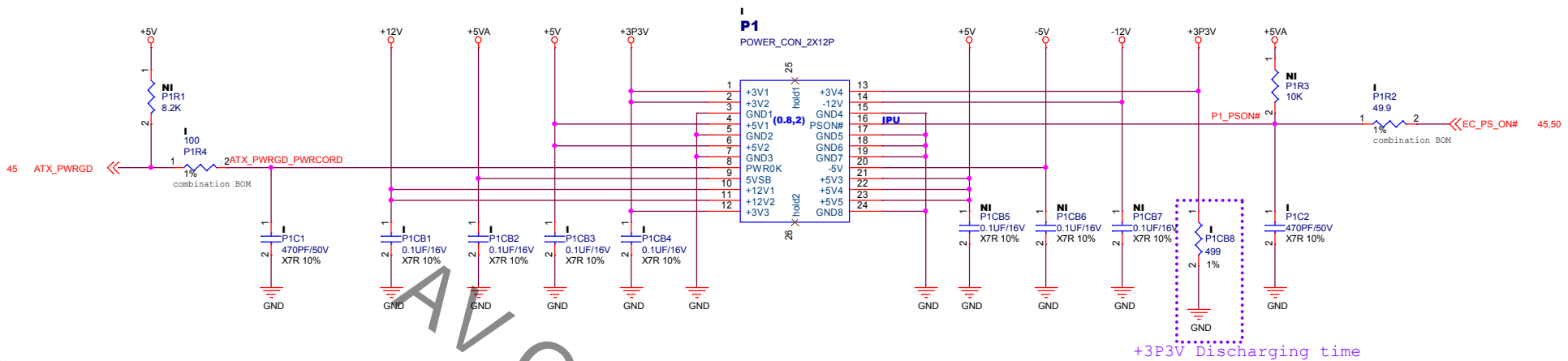
PROTO XDP2



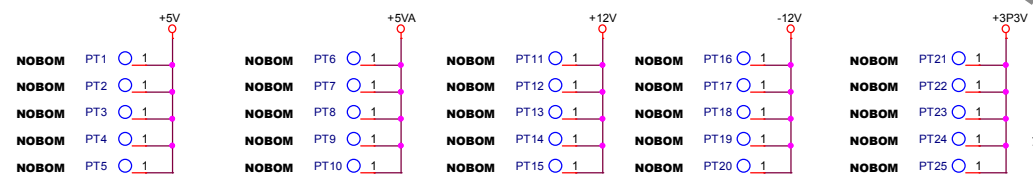
NOTE:
Place SPI MOSI 0 ohm near PCH

NOTE:
Place SPI_I02 0 ohm near PCH

ATX POWER_24P SUPPLY CONNECTOR

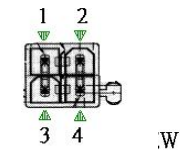
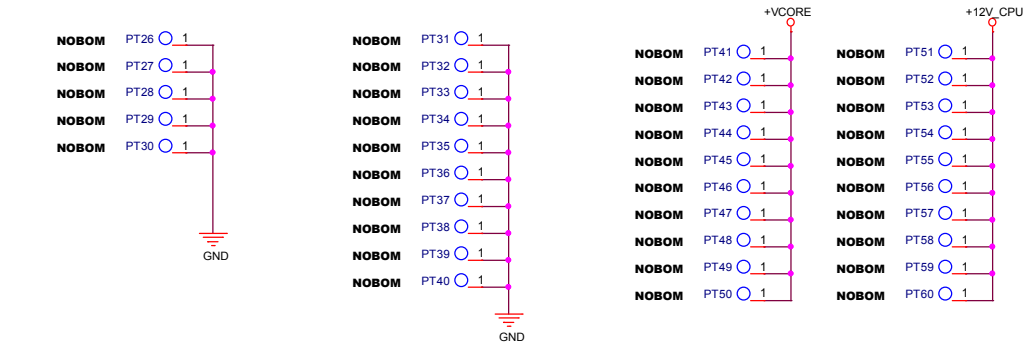


TOP SIDE VIEW



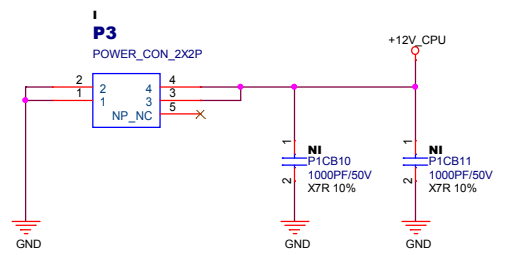
Nodes related to different power planes

Node	Goal Q'ty
+5V	5
+5VA	5
+12V	5
-12V	5
+3V	5
+Vcore	10
+GND	15
+12V_CPU	10



TOP SIDE VIEW

VRM POWER_4P SUPPLY CONNECTOR



5

4

3

2

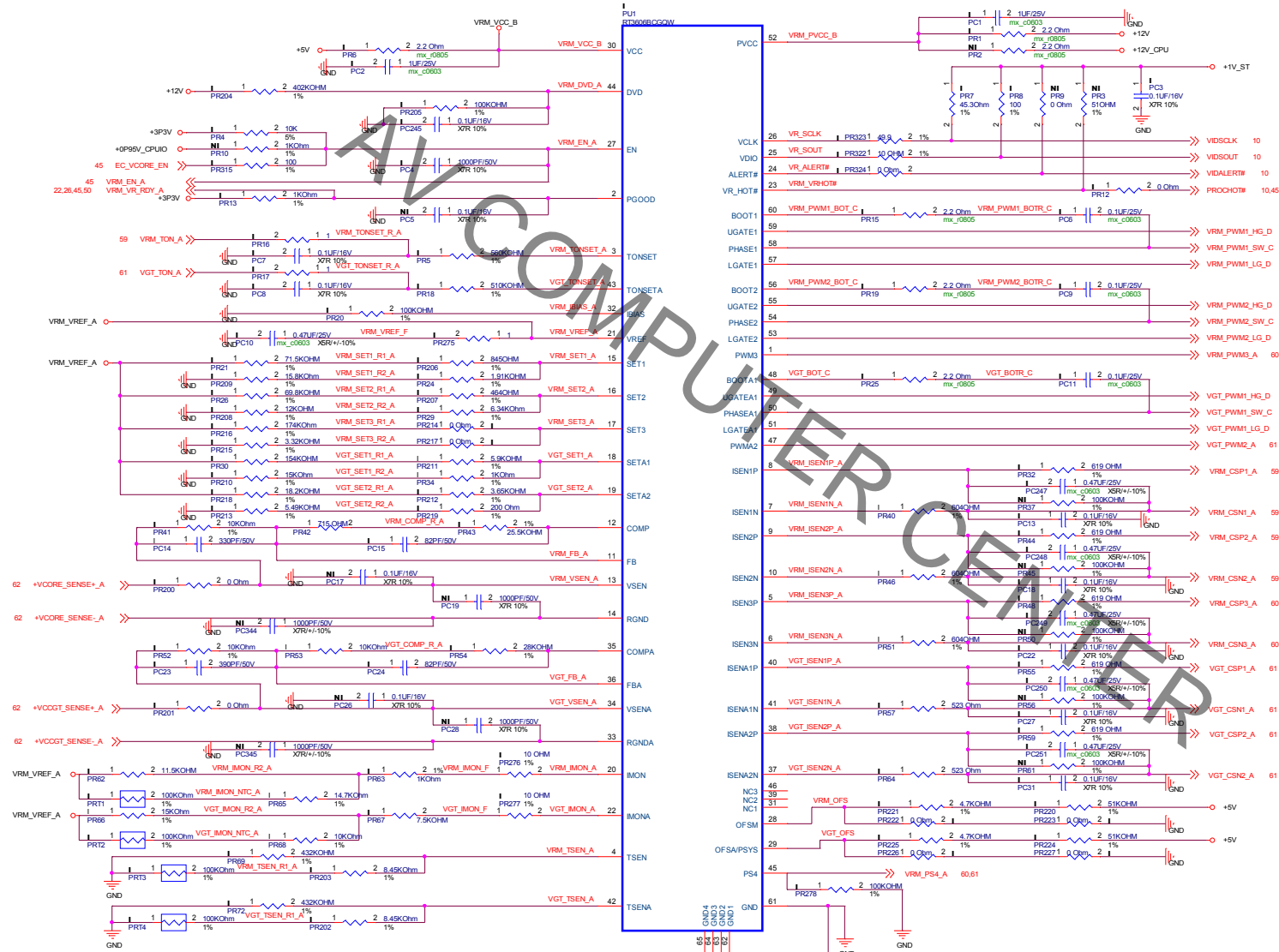
1

+VCORE

I_{max}=1.2A
I_{max}=1.00A
I_{tdc}=79A
LL=2.1m ohm
F_{sw}=300kHz
OC_P=133A
V_{ripple}=Intel spec

+VGT

I_{max}=5.1A
I_{max}=5.1A
I_{tdc}=37A
LL=3.1m ohm
F_{sw}=300kHz
OC_P=88A
V_{ripple}=Intel spec



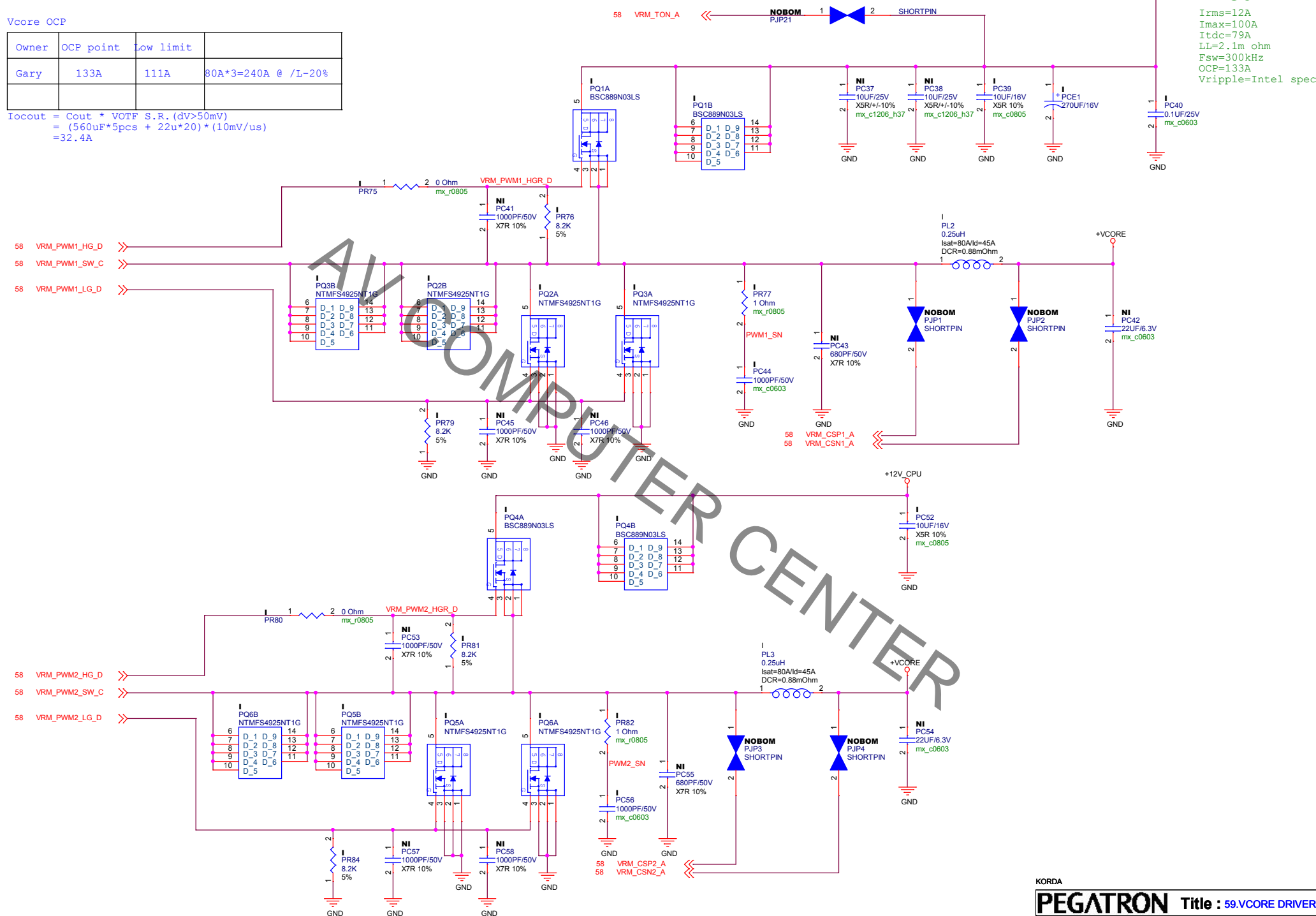
KORDA

PEGATRON Title :58.VCORE & VGT CONPEGATRON CORPORATION Engineer: Hemine HeSize Project Name **IPMKL-KD** Rev R1.00

Date: Friday, October 21, 2016 Sheet 58 of 70

Owner	OCF point	Low limit	
Gary	133A	111A	80A*3=240A @ /L-20%

```
58 VRM_PWM1_HG_D >>
58 VRM_PWM1_SW_C >>
58 VRM_PWM1_LG_D >>
```



```
Irms=12A
Imax=100A
Itdc=79A
LL=2.1m ohm
Fsw=300kHz
OCP=133A
Vripple=Intel spec
```


NB 5P

Owner	OCP point	Low limit	
Gary	88A	82A	80A*2=160A @ /L-20%

$$Tocout = Cout * VOTF \text{ S.R. (dV>50mV)}$$

$$= (560uF*5pcs + 22u*16)*(10mV/us)$$

$$= 31.52A$$

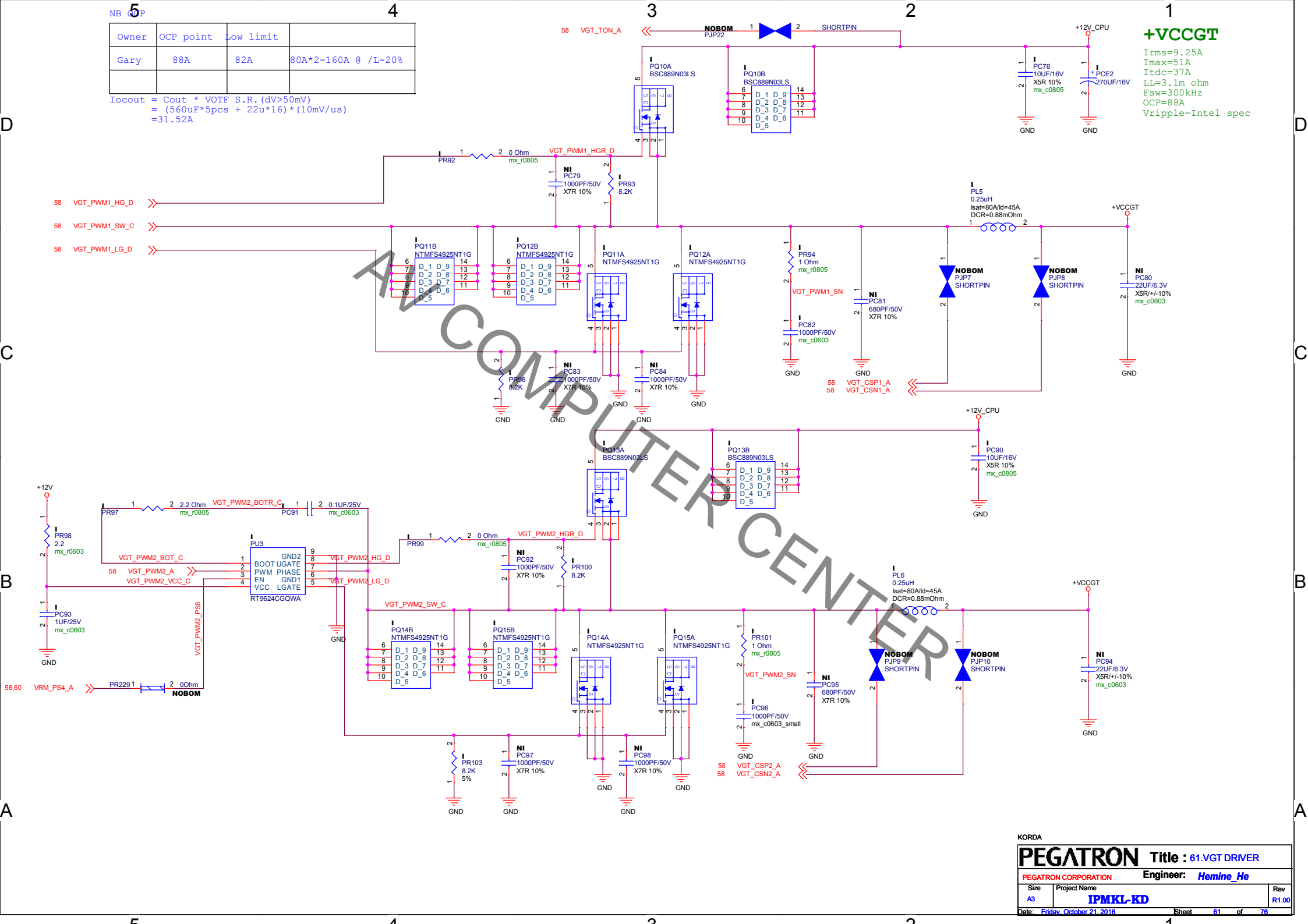
+VCCGT
 Irms=9.25A
 Imax=51A
 Itdc=37A
 LL=3.1m ohm
 Fsw=300kHz
 OCP=88A
 Vripple=Intel spec

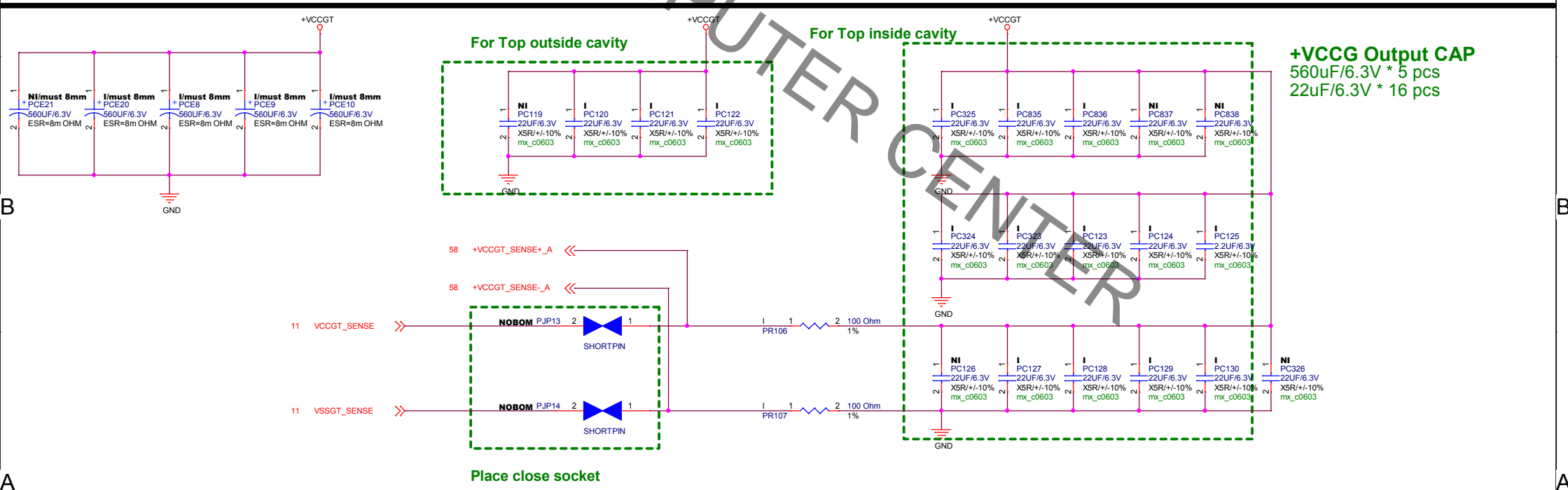
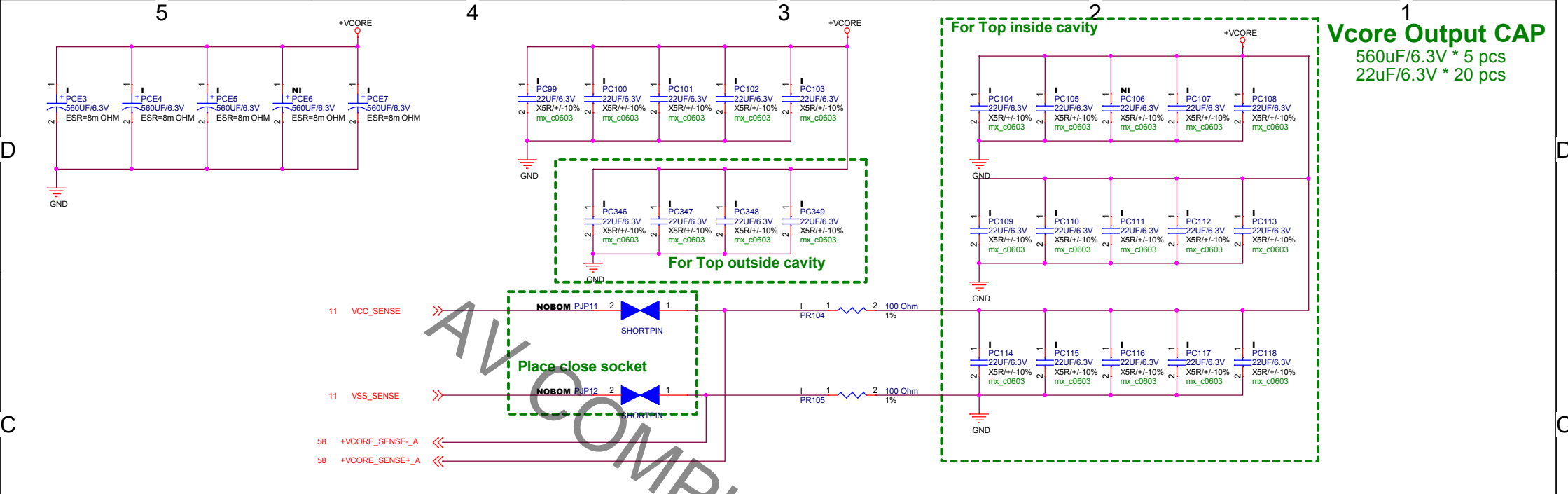
D

C

B

A

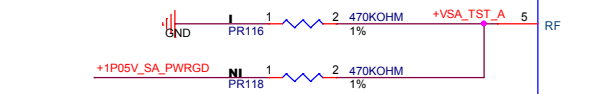
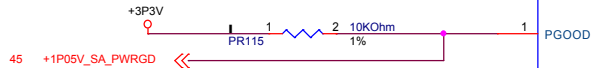
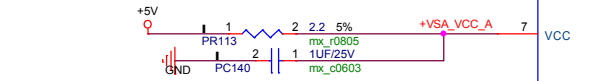
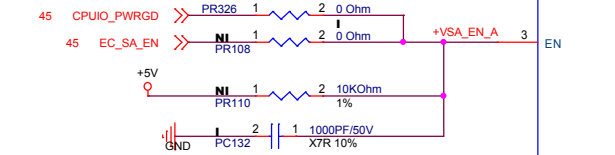




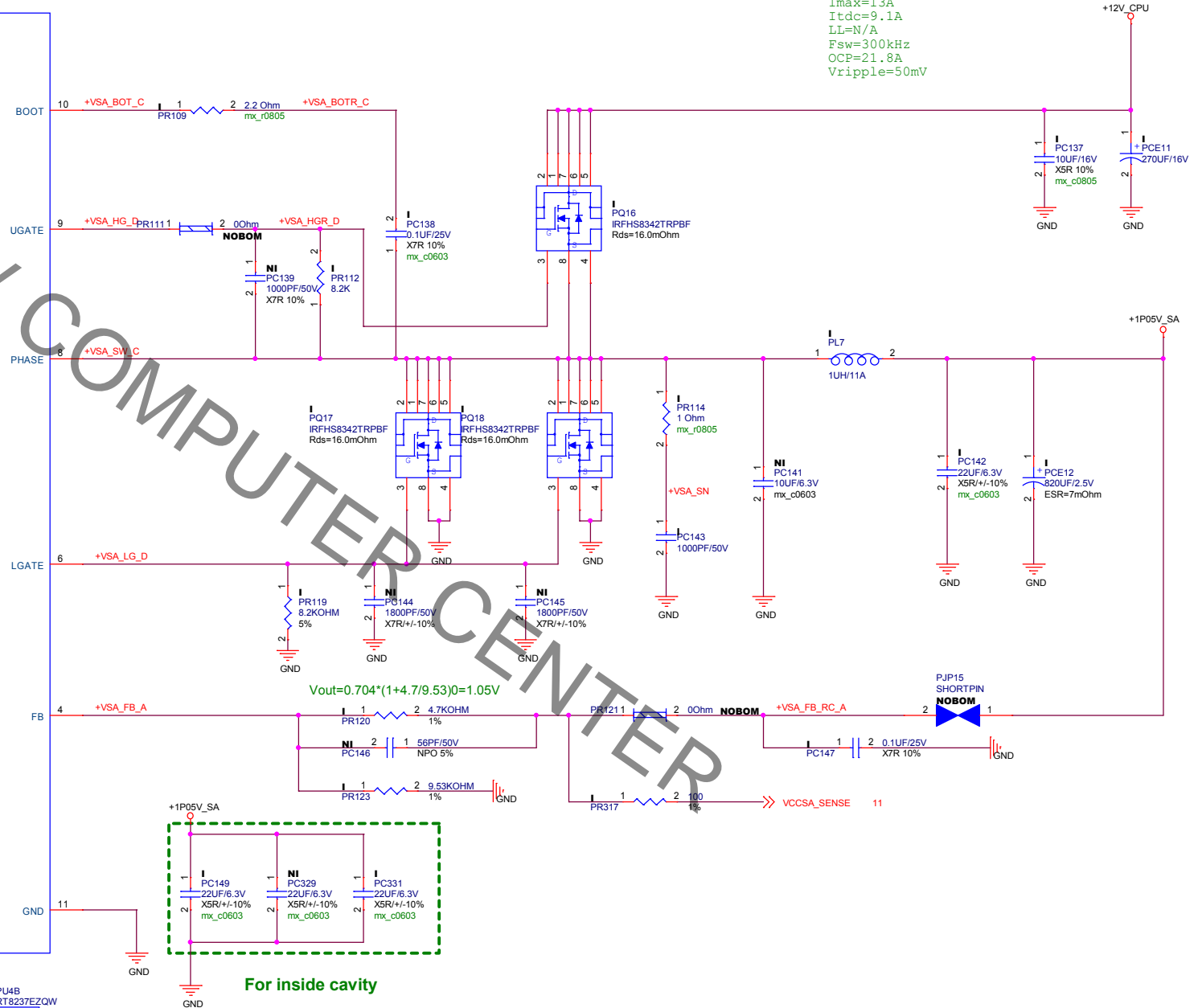
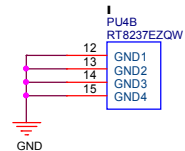
R _{RF} (kΩ)	Switching Frequency (kHz)
470kΩ	290
200kΩ	340
100kΩ	380
39kΩ	430

Note : For DEM, connect R_{RF} to GND; for CCM, connect R_{RF} to PGOOD.

Owner	OCP point (1.35V)	Low limit	High limit
Gary	21.8A@25deg 16A@105deg	NA	40A@-20%
Renton		NA	



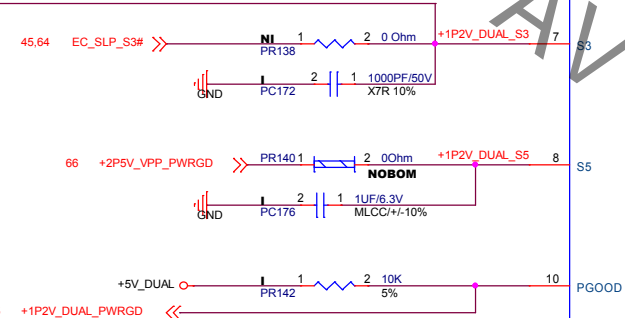
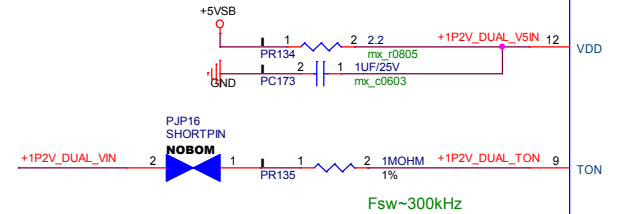
$$\text{OCP} = 200\text{k} \cdot 10^{-6} / (24\text{mohm} \cdot 1.4/2) / 8 + 2.1/2 = 18.2\text{A}$$

+1P05V_SA
—

```
Irms=2.35A
Imax=13A
It dc=9.1A
LL=N/A
Fsw=300kHz
OCP=21.8A
Vripple=50mV
```


Table 2. S3 and S5 truth table

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

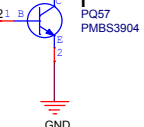
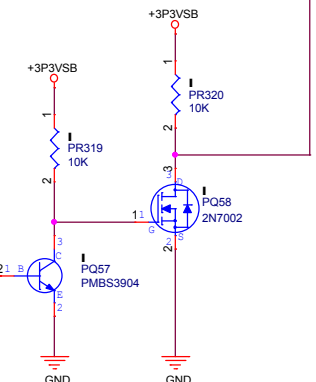
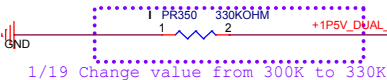


Owner	OCP point (1.35V)	Low limit	High limit
Gary	27.5A@25deg 19.64A@105deg	NA	40A@-20%
Renton		NA	

$$ILIMIT = (RLIMIT * 5\mu A) / (10 * R_{dson})$$

$$= (330k * 5\mu) / (10 * 8m * 1.4)$$

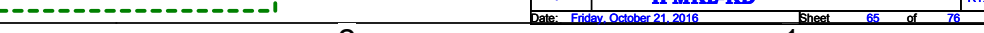
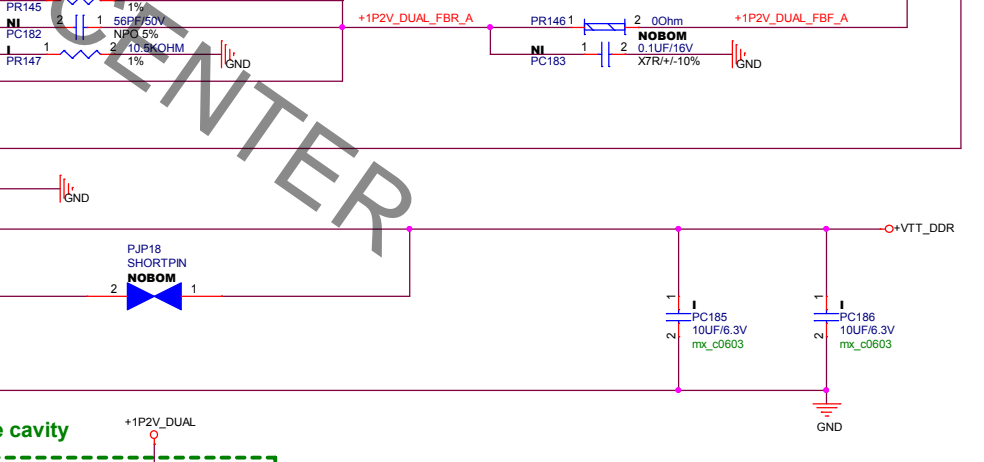
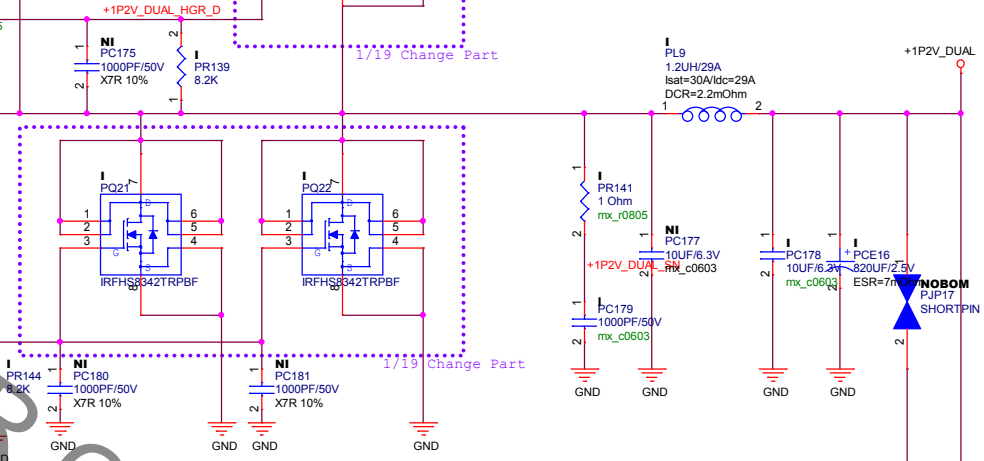
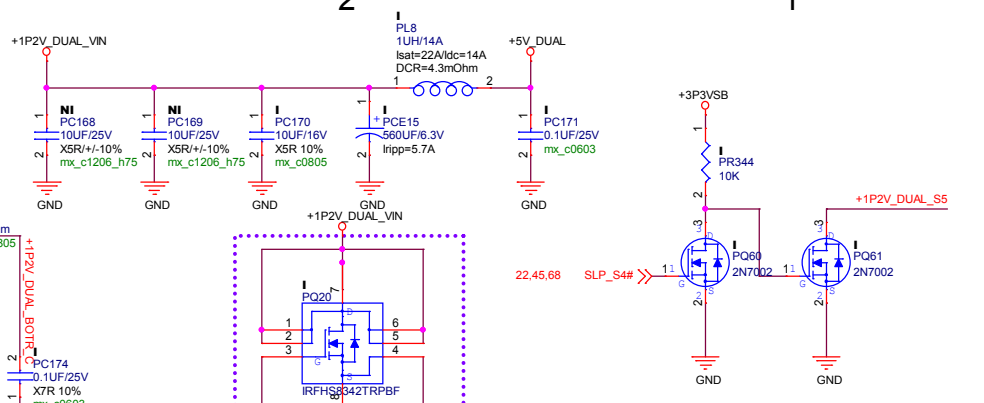
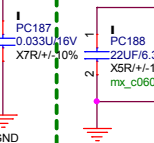
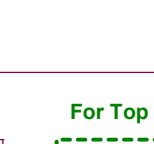
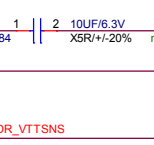
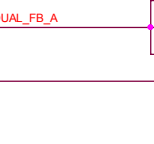
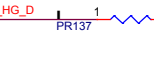
$$= 13.75A$$



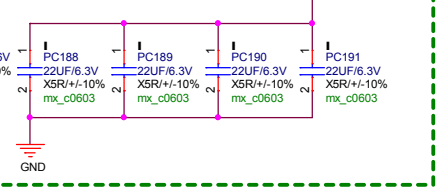
+1P2V_DUAL

Imax=7.8A
Tdc=5.5A
Irms=2.5A
LL=N/A
Vripple=50mV
Ocp=19.64A
Frequency=300K

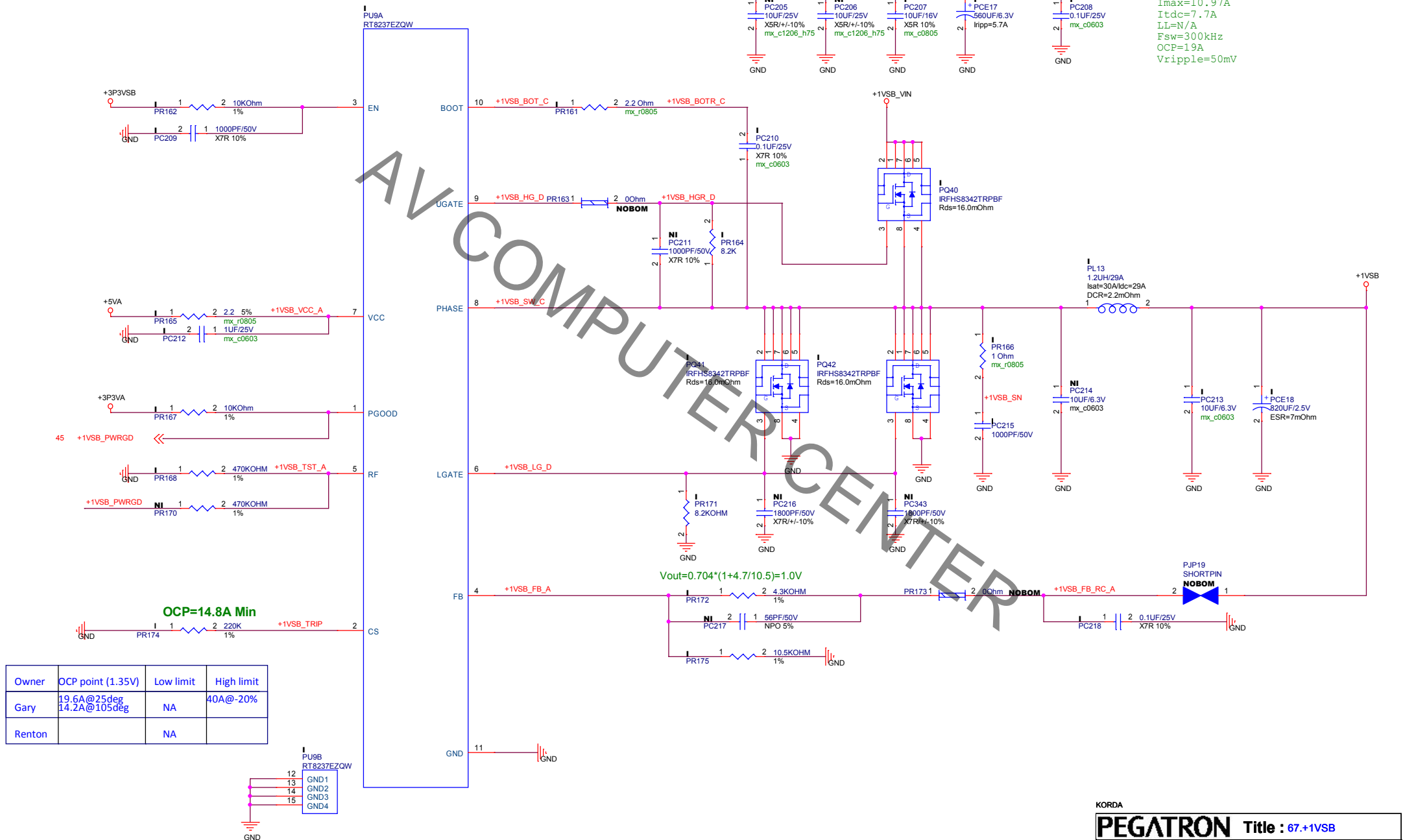
1/19 Change spec



For Top outside cavity



R_{RF} (k Ω)	Switching Frequency (kHz)
470k Ω	290
200k Ω	340
100k Ω	380
39k Ω	430



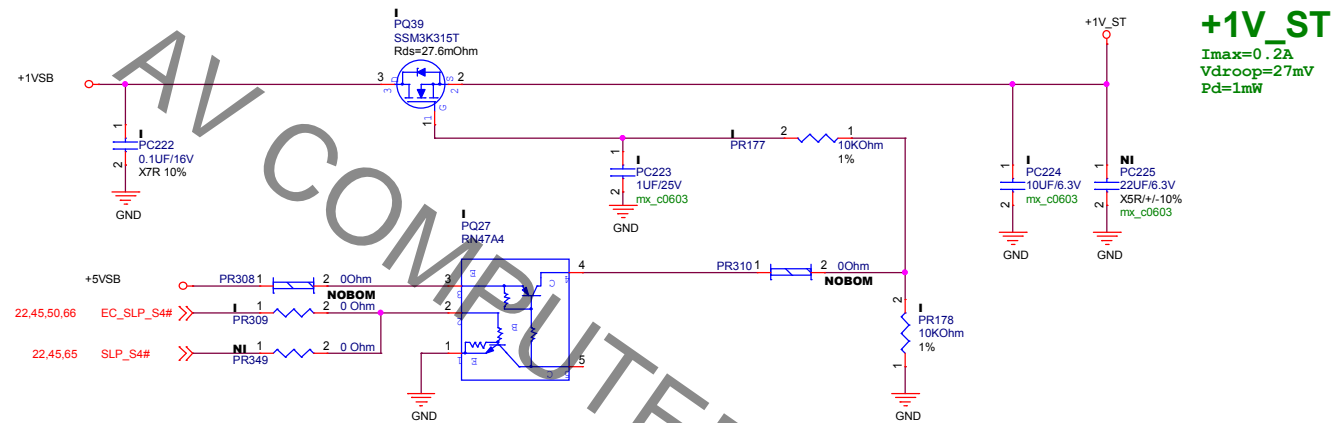
Owner	OCP point (1.35V)	Low limit	High limit
Gary	19.6A@25deg 14.2A@105deg	NA	40A@-20%
Renton		NA	

PEGATRON Title : 67.+1VSB

PEGATRON CORPORATION Engineer: *Hemine He*

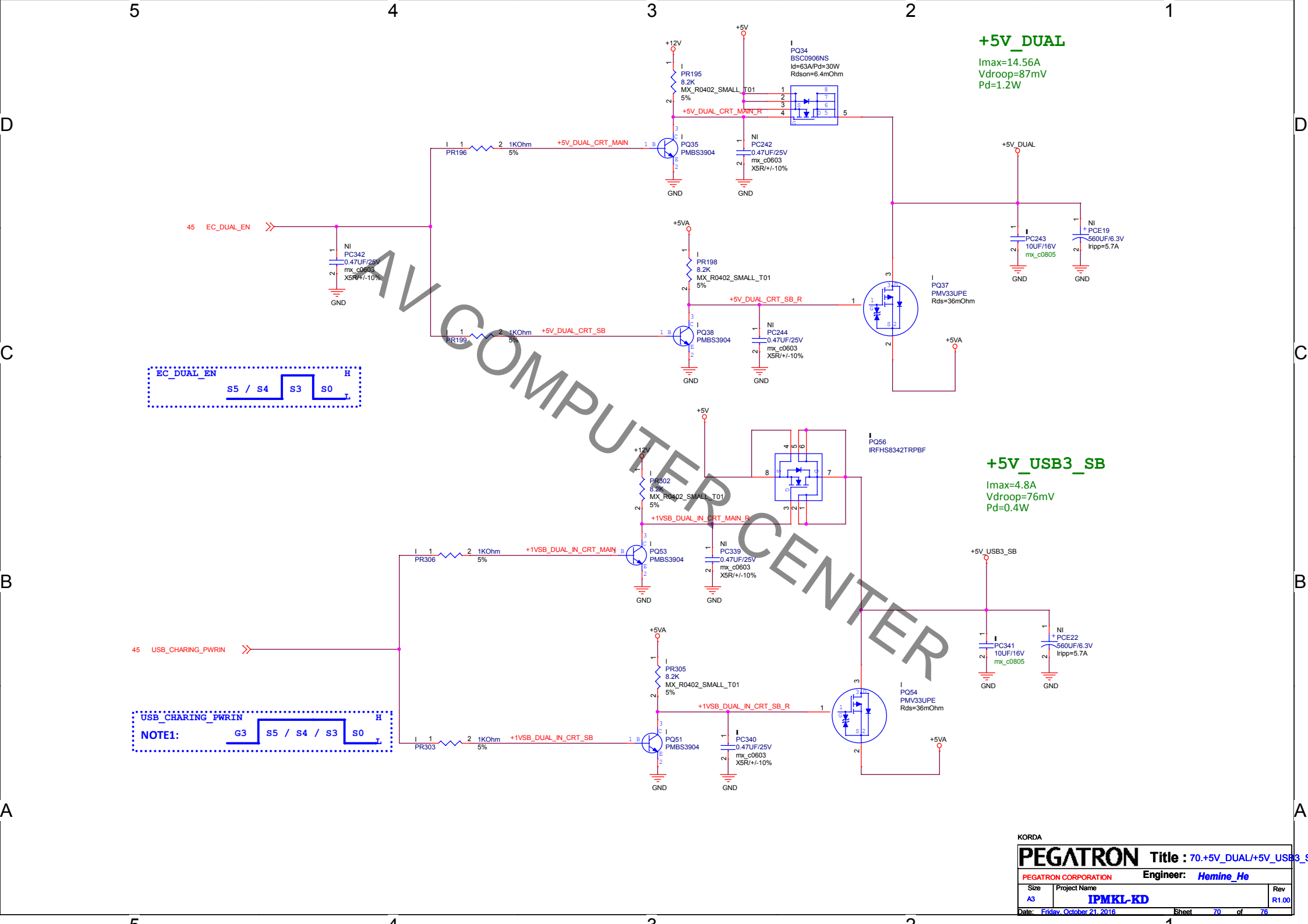
Size A3	Project Name IPMKL-KD	Rev R1.00
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Date: Friday, October 21, 2016 Sheet 67 of 76



KORDA

PEGATRON		Title : 68.+1V_ST	
PEGATRON CORPORATION		Engineer: <i>Hemine_He</i>	
Size A3	Project Name IPMKL-KD	Rev R1.00	
Date: Friday, October 21, 2016		Sheet 68 of 76	

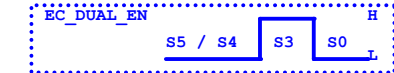


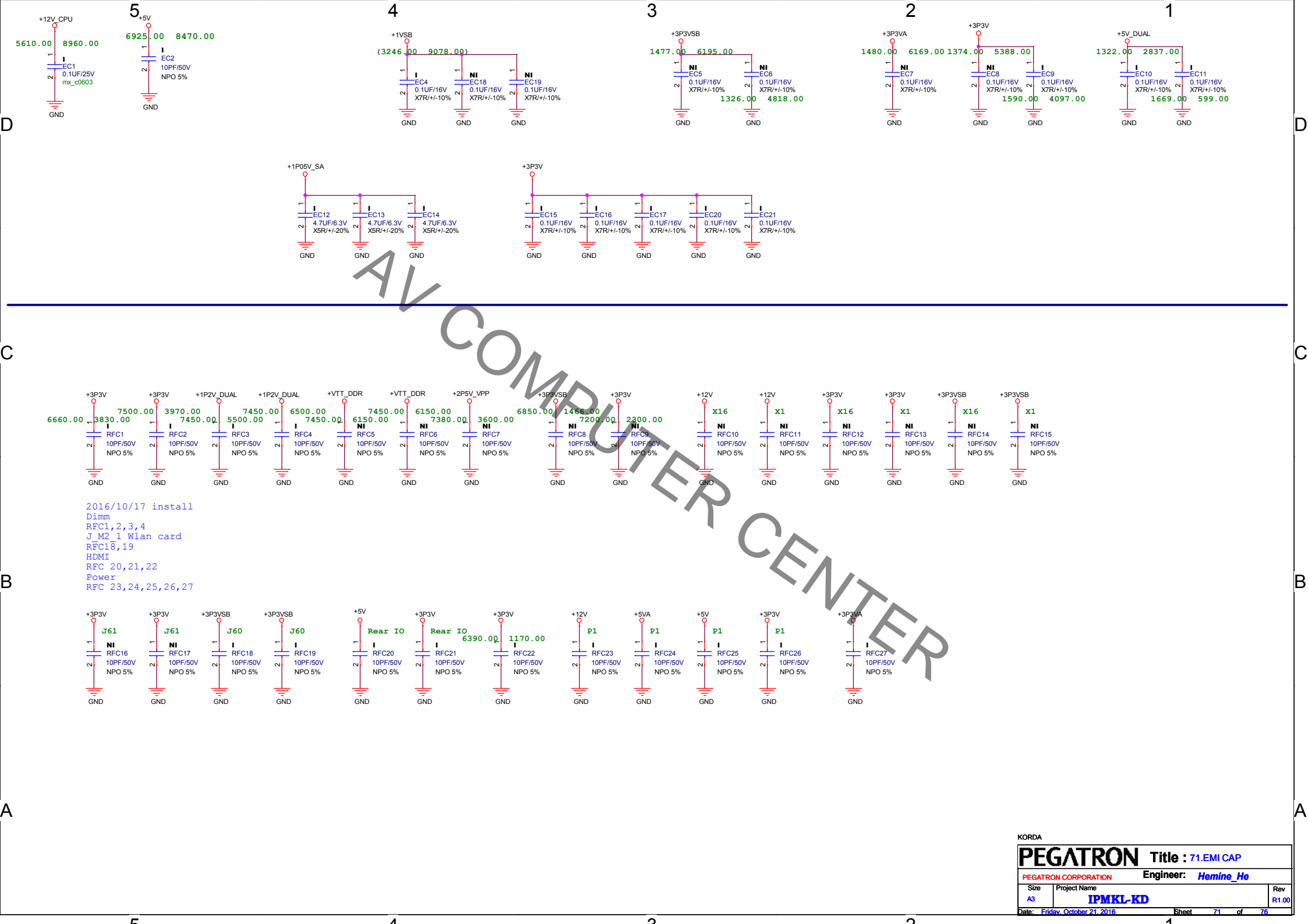
+5V_DUAL

Imax=14.56A
Vdroop=87mV
Pd=1.2W

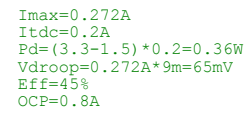
+5V_USB3_SB

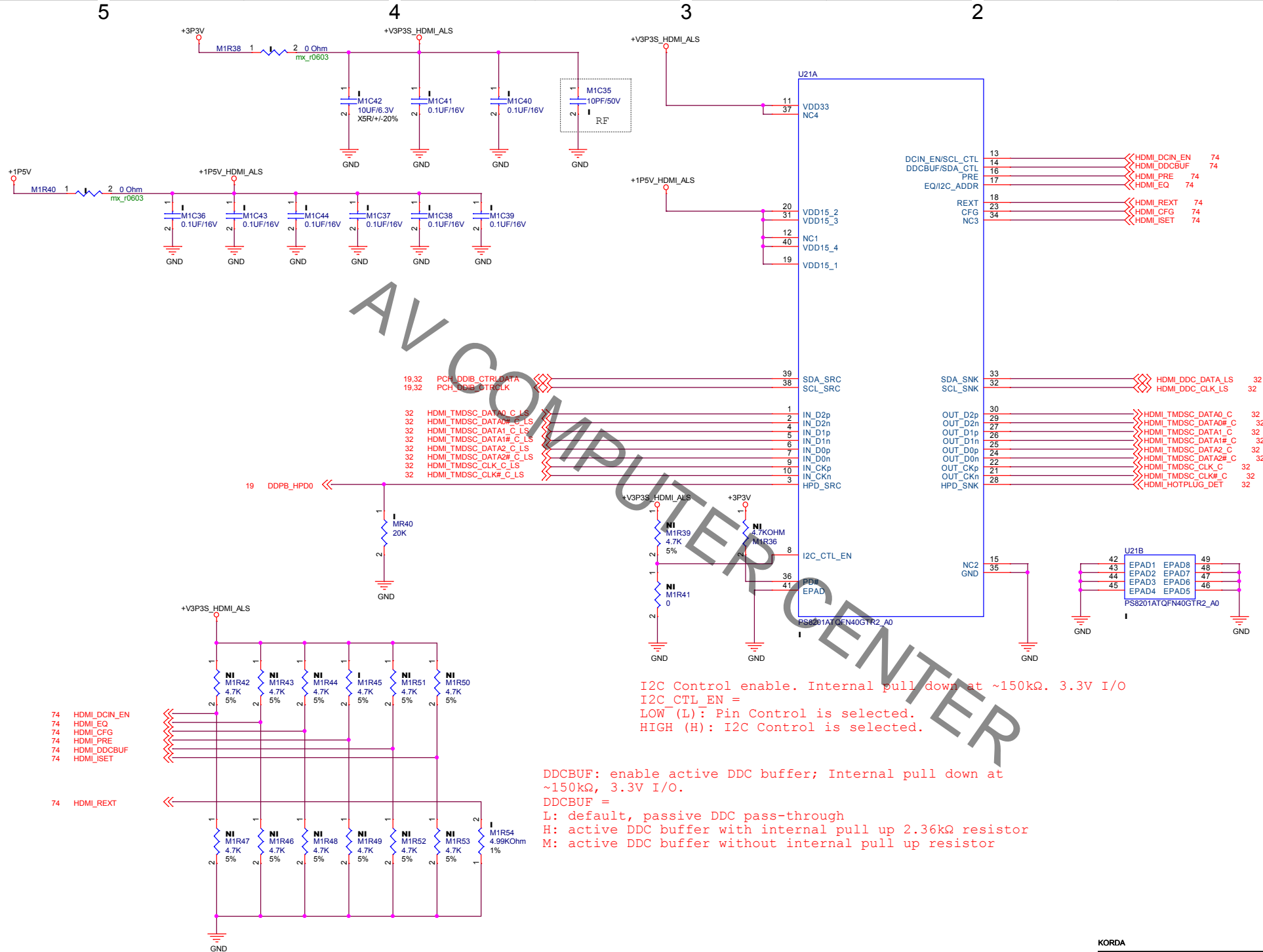
Imax=4.8A
Vdroop=76mV
Pd=0.4W





2016/10/17 install
Dimm
RFC1,2,3,4
J_M2_1 Wlan card
RFC18,19
HDMI
RFC 20,21,22
Power
RFC 23,24,25,26,27





1	+5V_TYPEC	+5V_TYPEC	2
3	D+	+5V_TYPEC	4
5	D-	U3_P56_SENSE#	6
7	GND	USB3_RX_P6	8
9	USB3_RX_P5	USB3_RX_N6	10
11	USB3_RX_N5	GND	12
13	CC2	CC1	14
15	GND	USB3_TX_P6	16
17	USB3_TX_P5	USB3_TX_N6	18
19	USB3_TX_N5		20

